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PIN SWITCH CIRCUITS INSTRUMENT FOR MICROSECOND VELOCITY MEASUREMENTS

BY HARRY E. CLEAVER

RESEARCH AND TECHNOLOGY DEPARTMENT

8 SEPTEMBER 1988

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The Pin Switch Circuits instrument combines signals generated by its 10-pin switch probe circuits into one coded output signal for recording on tape recorders on oscilloscopes. It has an internal test circuit for checking system performance and display generation purposes. The instrument plugs into a single-width compartment of the Tektronix TM500 Series Instrumentation Mainframes.

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FOREWORD

This document describes the operation and construction of the PIN SWITCH CIRCUITS instrument that is used with ionization pin probes in DDT studies by the Detonation Physics Branch. The document serves as the owners/operators manual and contains detailed information that can be used to service the instrument should the need arise, or even to construct another duplicate instrument.

Company and trade names used in this document are for technical information purposes only. Neither endorsement nor criticism is intended.

The contribution of Nicholas Vogle in constructing the instrument assembly is sincerely appreciated.

Approved by:

KURT F. MUELLER, Head
Energetic Materials Division

CONTENTS

ILLUSTRATIONS

ILLUSTRATIONS (Cont.)

TABLES

CHAPTER 1

INTRODUCTION

Various designs of pin switch circuits have been used for decades to mark the arrival of an event at a point in space for velocity of propagation studies. A pin switch circuit is simply a charged capacitor whose discharge through a monitor resistor is triggered when an event interacts with a pin switch probe. The probe can be any device whose response to the event is to simulate an electrical switch closure in order to discharge the capacitor. Velocity measurements are made by measuring the time interval required by the triggering event to travel the distance between two pin switch probes placed a preselected distance apart. One velocity measurement data point is obtained using two pin switches and recording the time interval between the signals on an electronic counter or oscilloscope. In real applications, a number of pin switch circuits are used and the time intervals between successive signals are measured. Any number of pin switches can be employed as long as some practical means is available to record all the time intervals. An often used technique, and the one used in this instrument, is to encode each pin switch signal with identifying characteristics, mix the signals together, and record them on a single channel of an oscilloscope or tape recorder.

The PIN SWITCH CIRCUITS instrument combines 11 pin switch circuits into a module that plugs into any Tektronix TM500 Instrumentation Series Mainframe. The front panel is shown in Figure 1-1 and the interior of the box showing the printed circuit board construction is displayed in Figure 1-2. The instrument is used primarily with coaxial ionization probes as the pin switch devices in explosion dynamics studies. Each of the 10 numbered circuits generates a signal having distinctly individual amplitude and polarity characteristics for purposes of probe identification. These ten signals are mixed to produce a single output signal appearing on the SIGNAL OUTPUT connector for recording on an oscilloscope. A test pattern displaying the coding used for all ten circuits is shown in Figure 1-3. One independent circuit is provided to generate a preevent trigger pulse, if needed, for the recording device. The output signal for this circuit appears on the TRIGGER OUTPUT connector and is shown in Figure 1-4. The signals in Figures 1-3 and 1-4 were captured on a Nicolet 4094 digital storage oscilloscope and plotted on a HP 7470A X-Y plotter.

An internal test system can be connected to all eleven pin switch circuits for self checking the instrument performance, for aid in adjusting the oscilloscope control settings during setup, and for testing probe continuity. Pressing any one of the numbered switches or the ALL switch on the 12 button TEST keyboard shown in Figure 1-1 will automatically connect the test system to the pin switch circuits and run the test. Once any one of these TEST switches is pressed, the test system remains connected to the pin switch circuits until the END switch is pressed causing the test system to be turned off. Pin switch circuits may be checked individually by pressing the

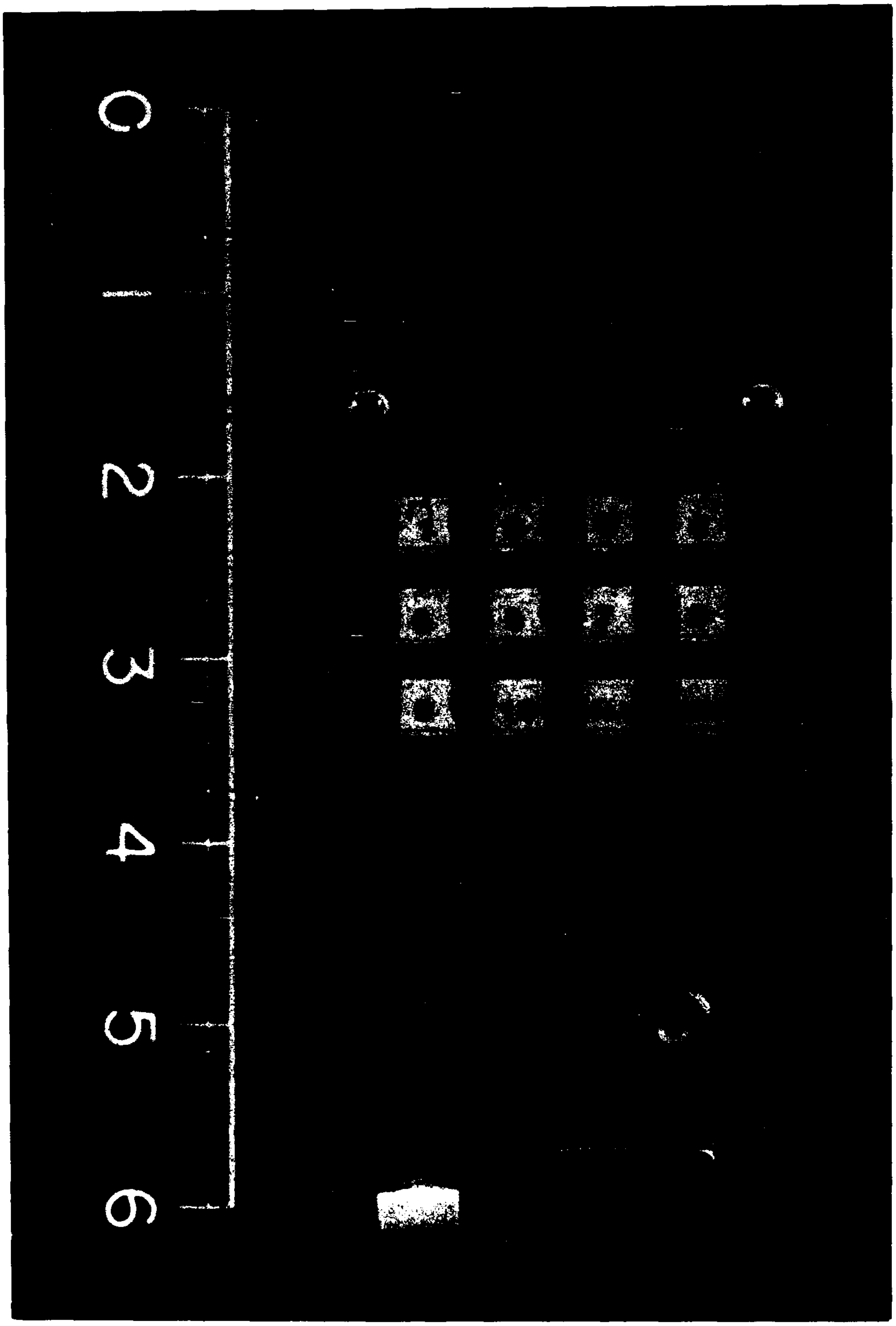


FIGURE 1-1. PIN SWITCH CIRCUITS FRONT PANEL

FIGURE 1-2. INSTRUMENT INTERIOR

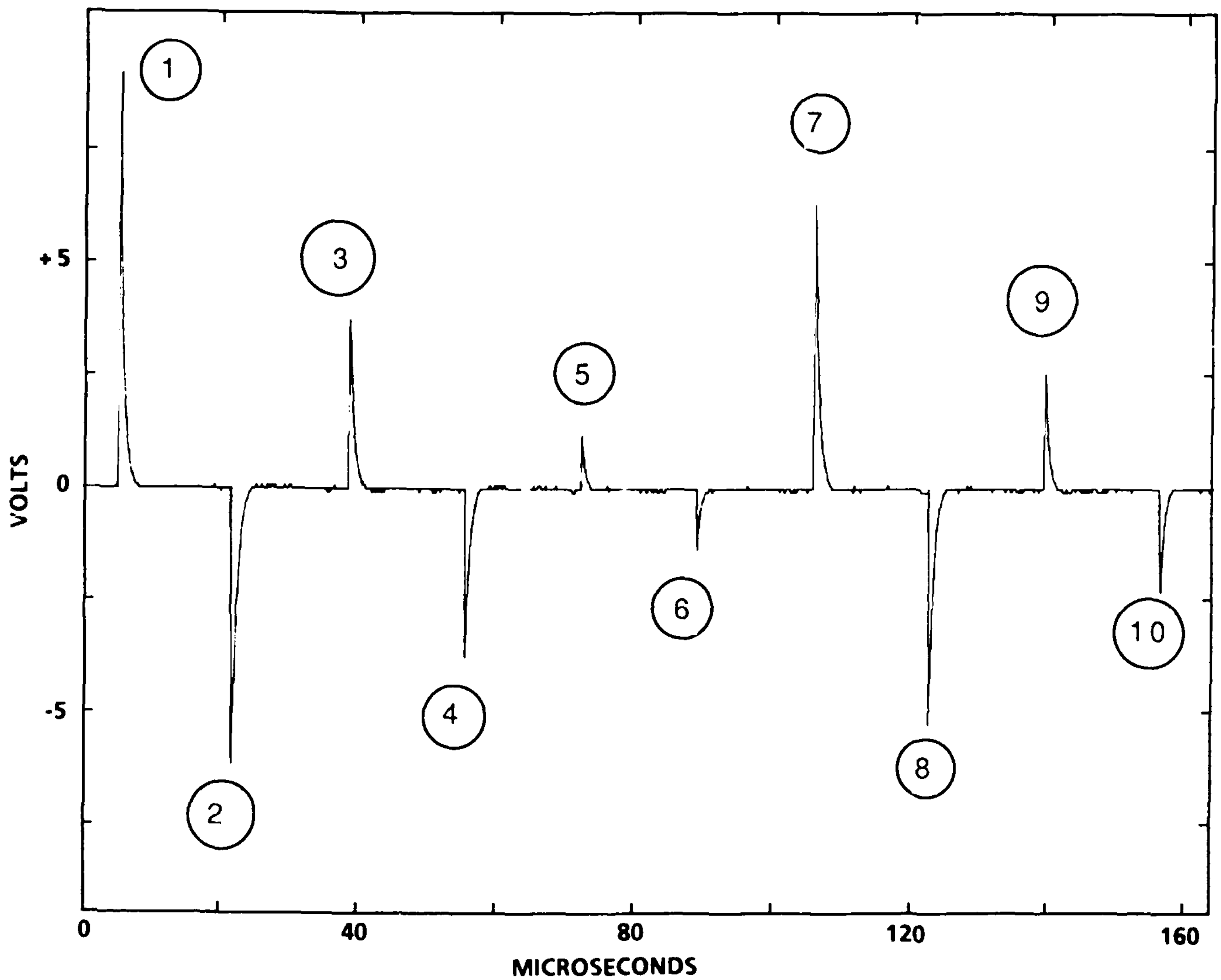


FIGURE 1-3. TEST SIGNAL DISPLAY USING "ALL" TRIGGERING

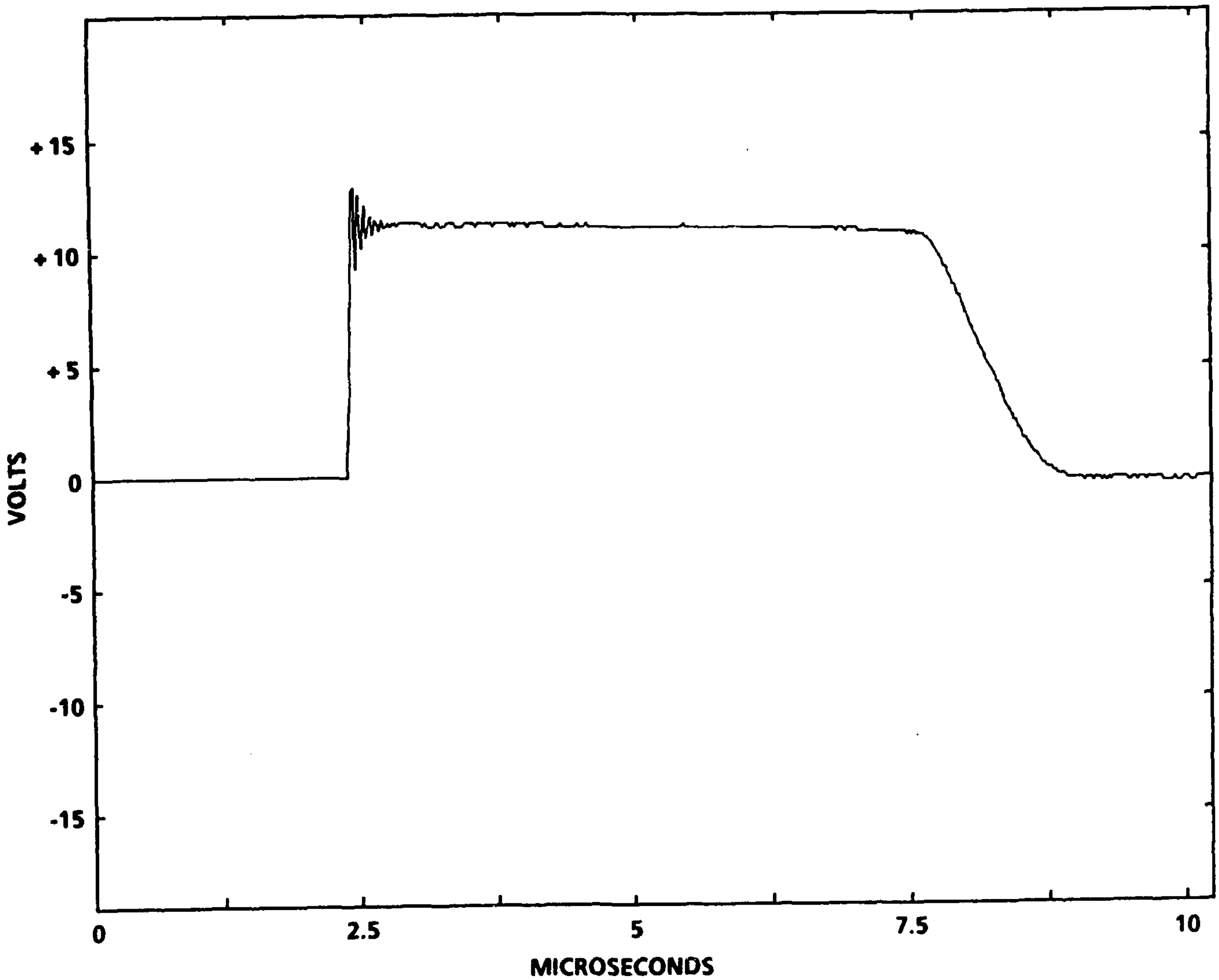


FIGURE 1-4. TRIGGER PROBE OUTPUT SIGNAL

desired circuit number on the TEST keyboard while viewing the oscilloscope trace for the corresponding signal display characteristics. Pressing the ALL switch starts an oscillator driven system that triggers all 10 pin switch circuits in sequence from 1 to 10 approximately 18 microseconds apart as seen in the oscilloscope trace in Figure 1-3. The ALL test circuit, for purposes of generating an oscilloscope display only, also triggers the independent pretrigger pin circuit about 9 microseconds before the test pattern in Figure 1-3 is generated. The test circuit oscillator frequency and the pin switch signal capacitor values were selected to meet the requirements of an overall 200 microseconds experimental time frame. Other experimental time frames could require that these circuit components be changed accordingly in order to produce a suitable display.

Statically, pin switch circuits resemble an electrical open circuit, therefore, breaks (open circuits) in the probe cable connecting system cannot be detected or diagnosed from the instrument end of the cable. This also means that test signal displays, such as in Figure 1-3, can be generated without the probes being connected to the instrument. A disconnected probe cable will result in failure to record any data in an experimental test. To prevent this loss of data, a jumper wire has been placed across two pins in the connector on the cable that is attached directly to the pin switch probes. When the probe cable is connected to the PIN SWITCH CIRCUITS instrument, and when the TEST system is off, the jumper wire completes a circuit so that the READY indicator light goes ON and +12 volts dc is applied to the READY connector for use with a remote monitor station. No positive READY status indication is possible if the probe cable is inadvertently left disconnected. When the probe cable is connected to the instrument, short circuit conditions in either the probes or cable can be detected by the absence of a signal or signals in the test display patterns.

In summary, the specifications of the PIN SWITCH CIRCUITS instrument are;

1. 10 pin switch circuits coded into one output signal
2. an optional pretrigger signal
3. an internal test/display system for a 200 microsecond span
4. local and remote READY status indicator
5. single-width module for Tektronix TM500 mainframes

CHAPTER 2

OPERATING INSTRUCTIONS

A diagram of the test setup of the pin switch circuit experiment is show in Figure 2-1. During the setup procedures, all probe cables going into the bombproof chamber are disconnected from the instrumentation and plugged into a safety ground system. Plug the PIN SWITCH CIRCUITS instrument into a Tektronix TM500 Instrumentation Series Mainframe. Connect the SIGNAL OUTPUT to the vertical amplifier input of an oscilloscope having a 1 Megaohm input impedance. Connect the READY +12V dc voltage indicator to the remote monitor. If the independent trigger pin probe is used, connect the TRIGGER OUTPUT signal to the EXTERNAL TRIGGER INPUT on the time base of the oscilloscope and set it for positive triggering as required for a +12 volt signal. Otherwise, set the sweep trigger circuit to POSITIVE INTERNAL TRIGGERING. Set the oscilloscope vertical amplifier to accept a +/- 10 volt signal and the time base sweep to cover 200 microseconds.

Test signals are generated in the PIN SWITCH CIRCUITS instrument by pressing any of the 11 TEST keyboard switches labeled 1 to 10 or the ALL switch. To establish proper instrument operating conditions, press the ALL switch to generate the complete probe signal display. All ten probe signals should be in view on the oscilloscope. Adjust the oscilloscope trigger level, beam intensity, and horizontal and vertical positioning controls for the desired display. When internally triggering, individual signals may be generated by using keyboard switches 1 through 10. ODD numbered circuits are checked using POSITIVE internal triggering; EVEN numbered circuits are checked using NEGATIVE internal triggering. When instrument performance is verified, press the END TEST switch to turn off and disconnect the test circuit.

Before the 10 conductor cable is connected to the pin switch probes, its condition can be tested for electrical continuity by connecting it to the instrument via the transfer box and tapping each wire to the signal ground return while checking the oscilloscope for the correct signal display. The TRIGGER pin cable can be tested in the same way if it is used.

When the experimental test model is in place and all is ready for firing the test as shown in Figure 2-1, disconnect the probe cable from its safety grounding plug and connect it to its matching instrument cable plug on the transfer box. If the TRIGGER pin probe circuit is used, disconnect the trigger pin cable from its grounding plug and connect it to its mating connector on the transfer box. Note that when the energized instrument is connected to the charge, minus 4 volts dc is applied to the probes embedded in the explosive. If the TEST circuit is off, the READY light will turn on and +12V dc will be applied to the READY monitor connector.

Once the pin switch probes are connected to the instrument, check the oscilloscope display using the ALL switch to verify that all 10 signals are in

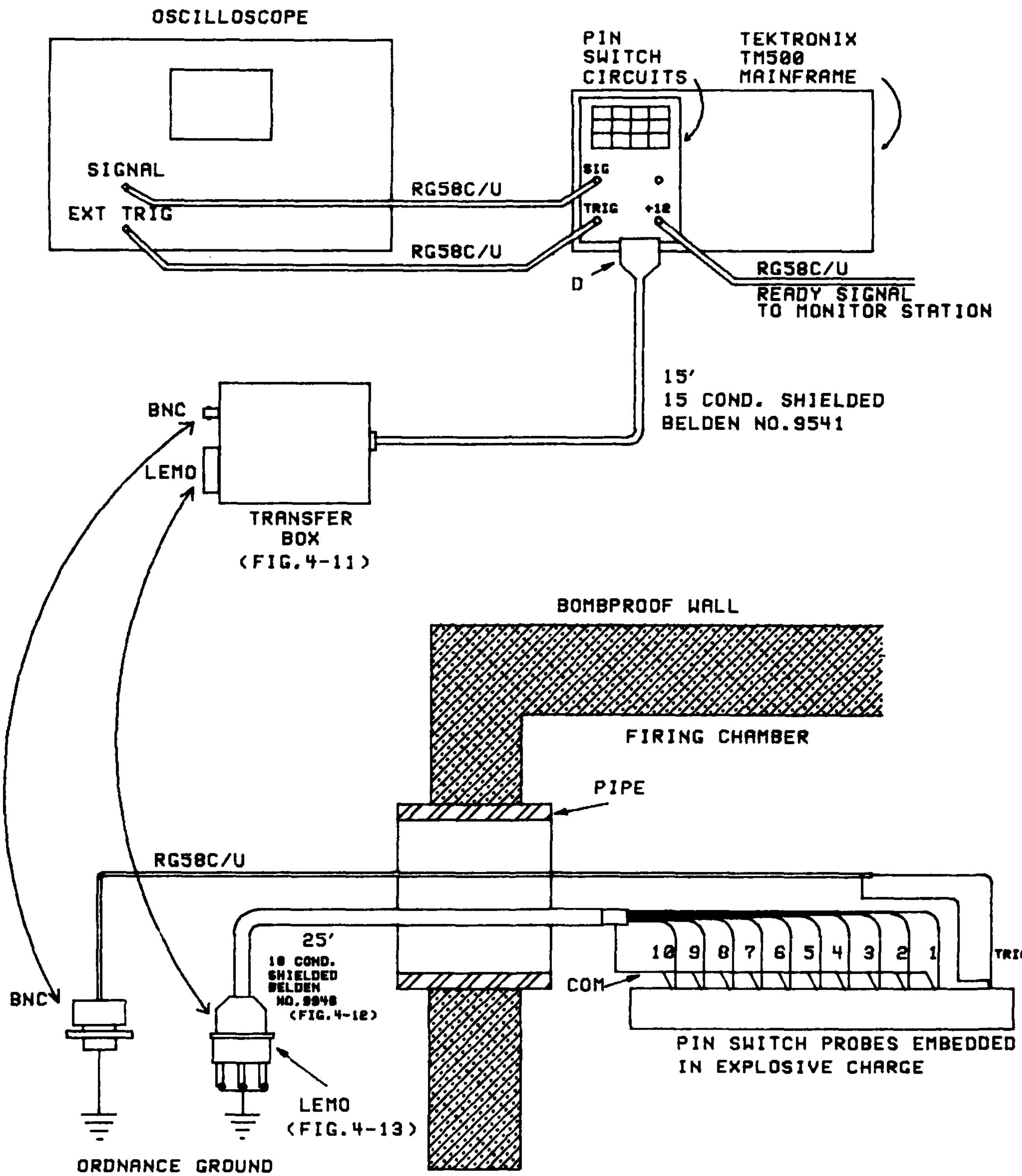


FIGURE 2-1. INSTRUMENTATION SETUP

the display. Signals having reduced amplitude or that are missing altogether indicate problems of leakage or shorting in the probe cable assembly and will require troubleshooting the assembly. Next, adjust the oscilloscope TRIGGER LEVEL control as desired by (1) using one of the individual circuit TEST keyboard switches as a trigger reference source when internally triggering or (2) using the ALL TEST switch when externally triggering.

When all final checks for proper display and all trigger level adjustments are over, press the END TEST switch to disconnect the TEST circuit. Verify that the READY status indicators are ON. Set the oscilloscope for SINGLE SWEEP operation, open the camera shutter, if used, and fire the test experiment.

CHAPTER 3

THEORY OF OPERATION

The simplest form of a pin switch circuit is shown in Figure 3-1(A). There are two basic requirements of a pin switch circuit. The first is to generate a signal with a fast rise time and a narrow pulse width in relation to the time intervals being measured. The second requirement is to have a long capacitor recharge time relative to the experimental time frame in order to prevent multiple signal generation caused by secondary restrikes on the pin switch probes.

The pin switch device, represented schematically as a switch with associated resistance Rs, can be any device that reacts like a switch closure to events such as pressure change, gaseous ionization, metallic contact, etc. In the initial state of the circuit, capacitor C is charged to the supply potential V through a high resistance R1. When the event closes the pin switch, capacitor C discharges through the switch resistance Rs and the load resistor R2. The charging resistance of R1 is large enough to keep the capacitor from recharging to any appreciable level during the time frame of the experiment. Resistance of the load R2 is kept small, usually around 50 ohms. The value selected for capacitor C is dictated by the requirements of output signal pulse width. The output signal is a voltage spike with an exponential decay developed across R2. The negative supply voltage shown produces a positive going output signal; a positive supply produces a negative going output signal. Note that the capacitor discharge time constant is (R2+Rs)C and the discharge voltage is developed across Rs and R2. In most cases, but not all, the effect of the pin switch resistance is small and can be neglected.

When using a number of pin switch circuits and wanting to encode their signals with different voltage amplitudes, circuits of the type in Figure 3-1(B) are used. Ignoring the switch resistance for the moment, the discharge of capacitor C appears across R2 and R3. The sum of the two resistances R2 and R3 is held constant in each circuit in order to maintain the same discharge time constant. The ratio of the two resistances is varied from circuit to circuit to change the amplitude of the voltage appearing across the output resistor R3. Pulse width coding can also be done in this circuit by changing the values of capacitor C from circuit to circuit. When a number of pin switch circuits are used, they are isolated from each other by diodes and their output signals are summed on a common output resistor as shown in Figure 3-1(B).

When ionization probes are used as the pin switch device, switch resistance Rs is the resistance of the ionized zone as it sweeps across the probe tip. In some cases this resistance can be large and variable enough to distort the output signal amplitude and time constant characteristics making it difficult to match a signal with its designated circuit number when

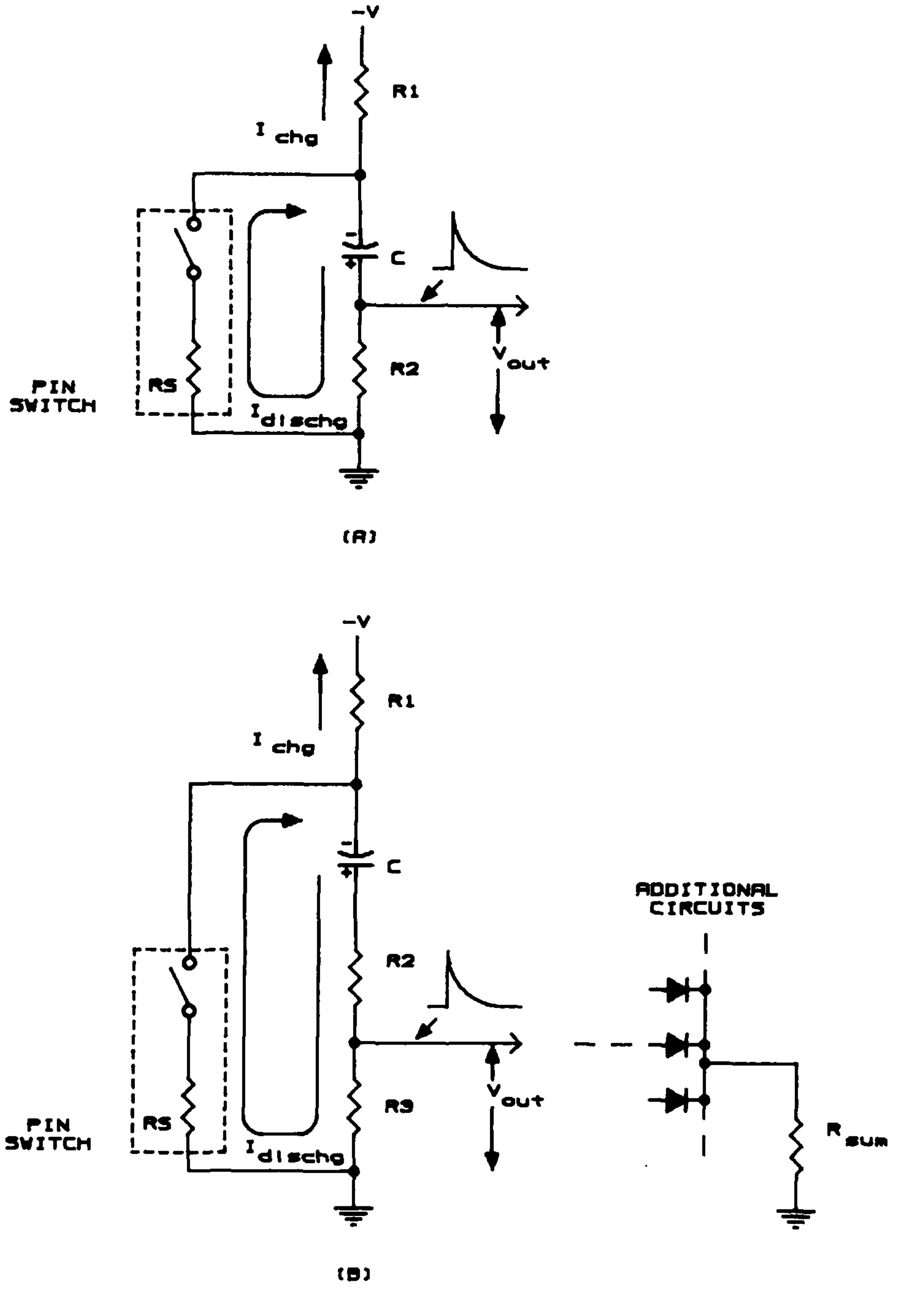


FIGURE 3-1. BASIC PIN SWITCH CIRCUITS

analyzing the composite output signal trace as recorded on the oscilloscope. The pin switch circuit shown in Figure 3-2 improves signal trace identification by eliminating output signal distortion caused by high switch resistance.

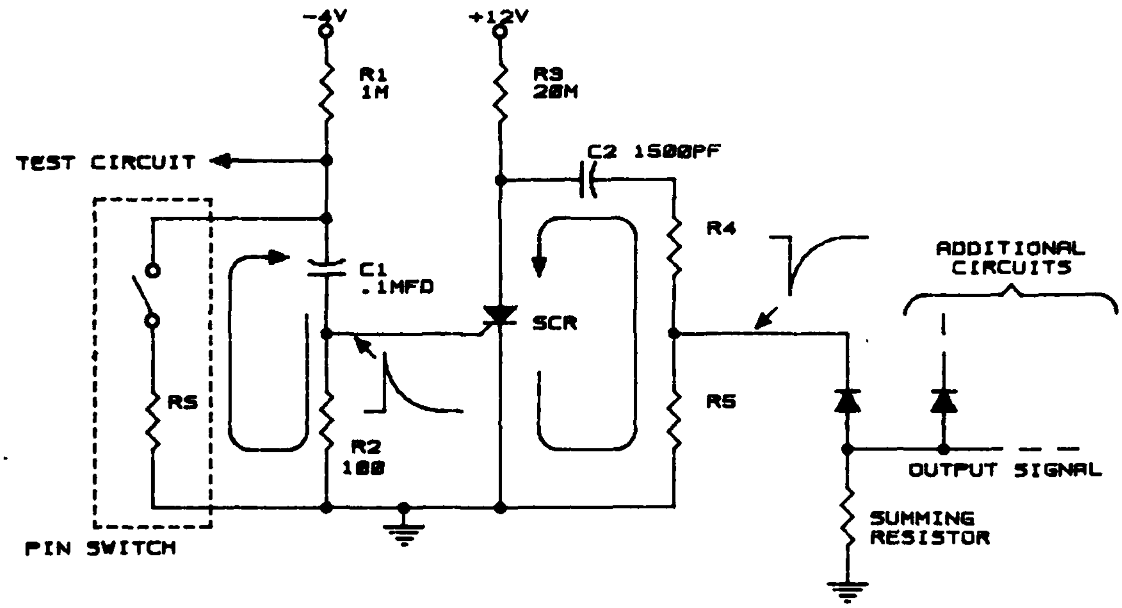
The circuit design in Figure 3-2 is the one used for all 10 probe circuits in the PIN SWITCH CIRCUITS instrument. The basic pin switch circuit, consisting of R1, C1, and R2, is used to trigger a silicon controlled rectifier (SCR). The output signal is generated as capacitor C2 discharges through the SCR and across R4 and R5. Pin switch resistance Rs is removed from the output signal generating path and is replaced by the dynamic resistance of the SCR. Dynamic resistance among SCRs is considerably more uniform and stable than the variable resistance presented by ionized zones in some test experiments; thus the output signals retain their waveform characteristics from one test to another. What is required is that the resistance of the ionized zone be low enough that sufficient voltage is generated across R2 to trigger the SCR.

In the initial state, capacitors C1 and C2 are charged to their respective supply voltages through R1 and R3. When the pin switch is closed by the arrival of the event, capacitor C1 discharges across R2 developing a positive voltage spike on the gate of the SCR. Triggered into conduction, the SCR dumps the charge stored in C2 across the R4 and R5 resistor chain. A negative going voltage spike is developed at the R4, R5, and diode junction. When the current discharged through the SCR drops below its holding value, the SCR turns off and C2 can begin to recharge. As already described, the output voltage amplitude is set by the ratio of R4 and R5, the pulse width by the capacitor C2 value, and the 1N914 diode provides circuit isolation. The table in Figure 3-2 lists the component values used in the 10 circuits to achieve the amplitude coding displayed in Figure 1-3.

All pin switch-SCR circuits were tested to determine what resistance in parallel with the pin switch probe and what resistance in series with the probe would cause the circuit to fail to trigger. Failure would be due to insufficient energy being delivered to the gate of the SCR to trigger it into conduction. Tests were performed using ten-turn variable resistance potentiometers connected to the end of the complete instrumentation cable assembly.

Parallel resistance paths across the probes, which would affect the voltage stored on C1, could be due to damage in the cable assembly or to conduction in the medium in which the probes are imbedded. Results of the parallel resistance leakage path test showed that all circuits worked down to a resistance of about 550k ohms. All circuits failed by about 470k ohms and below. As each circuit approached its failure point, the output signals showed a fairly abrupt 2 to 15 percent reduction in amplitude just before failure.

Series resistance effects appear when the probe circuit is triggered and might possibly be from a damaged cable assembly but most likely would be in the resistance appearing across the probe tip, such as the resistance in the ionization zone as it crosses the tip. All circuits worked with a series resistance, upon triggering of the probe, from zero up to about 550 ohms. Circuits 1 to 10 failed by 740 ohms; the TRIGGER pin circuit failed at 950 ohms. Again, when approaching failure,the circuits showed a fairly abrupt reduction in output signal amplitude, this time of 4 to 32 percent.



SCR = GA300, BY UNITRODE CORP

DIODE = 1N914

CIRCUIT NUMBER	1	2	3	4	5	6	7	8	9	10
R4 - OHMS	0	0	200	200	402	402	100	100	301	301
R5 - OHMS	499	499	301	301	100	100	402	402	200	200
RELATIVE PULSE HEIGHT	+5	-5	+3	-3	+1	-1	+4	-4	+2	-2

RN55D 1% METAL FILM RESISTORS

FIGURE 3-2. PIN SWITCH AND SCR CIRCUIT

In summary, these tests show that all circuits will work reliably with a parallel resistance down to 550k ohms and a series resistance in the probe connection up to 550 ohms.

Because the output signal from each of the 10 circuits is negative going, the means to get polarity encoding is incorporated into the signal output amplifier shown in Figure 3-3. An operational amplifier (op-amp) is used in a subtractor circuit configuration with the basic transfer equation of

$$E_{OUT} = \frac{R_8}{R_7}E_2 - \frac{R_6}{R_5}E_1$$

where E_{OUT} = output voltage
E_2 = voltage on the NON-INVERTING input
E_1 = voltage on the INVERTING input.

Negative going signals from the ODD numbered pin switch circuits applied to the INVERTING input of the op-amp are inverted and appear as positive going in the output display. Signals from the EVEN numbered circuits applied to the NON-INVERTING input of the op-amp are transmitted without inversion and retain their negative going characteristics. Gain or attenuation of the pin switch signals can be set by the ratio of the feedback resistors as seen in the equation. Thus the five ODD numbered pin switch signals are inverted in polarity and mixed with the five EVEN numbered signals to produce a single output signal as shown by the display in Figure 1-3.

The op-amp used in the mixer circuit is a Harris Semiconductor HA-2540. The pertinent characteristics of this amplifier are its gain-bandwidth product of 400 mHz, slew rate of 400 v/microsecond, settling time of 250 nanoseconds, and its minimum stable gain of 10. Because of these high speed characteristics, care had to be taken with the printed circuit board layout, component selection, and power supply decoupling in order to realize the amplifier's potential and keep it stable. The 10k and 100k resistors at the amplifier input set the gain to 10. Because the signals coming directly from the pin switch-SCR circuits would overdrive the amplifier at its gain of ten, they are attenuated by the 10k and 1k dividers before being applied to the amplifier inputs. Lead lengths to the amplifier were kept short, a single point ground was used, and the output signal is connected by a coaxial cable through an isolated ground BNC connector to the oscilloscope.

Tests were conducted to determine what was the signal propagation delay, and to determine if the propagation delay was the same for every pin switch circuit. Results of the test show that the propagation delay from the time the pin switch capacitor discharges through the SCR gate lead resistor to the peak of the output signal is about 50 nsec. No measurable differences were noted among the 10 circuits. Rise time of the output signal is about 25 nsec. The TRIGGER pin switch circuit signal, which does not go through the op-amp, showed about the same propagation delay and rise time (actually slightly faster) as well as some ringing at the leading edge.

The TRIGGER pin switch circuit, shown in Figure 3-4, was designed to provide an independent signal that can be used to trigger the recording device before the main 10 pin switch circuits will be triggered. Use of such an option has been an advantage in some past experiments when selecting a trigger from among the other ten probes could rot always guarantee that the probe selected would be the first one triggered. In use, the TRIGGER pin switch

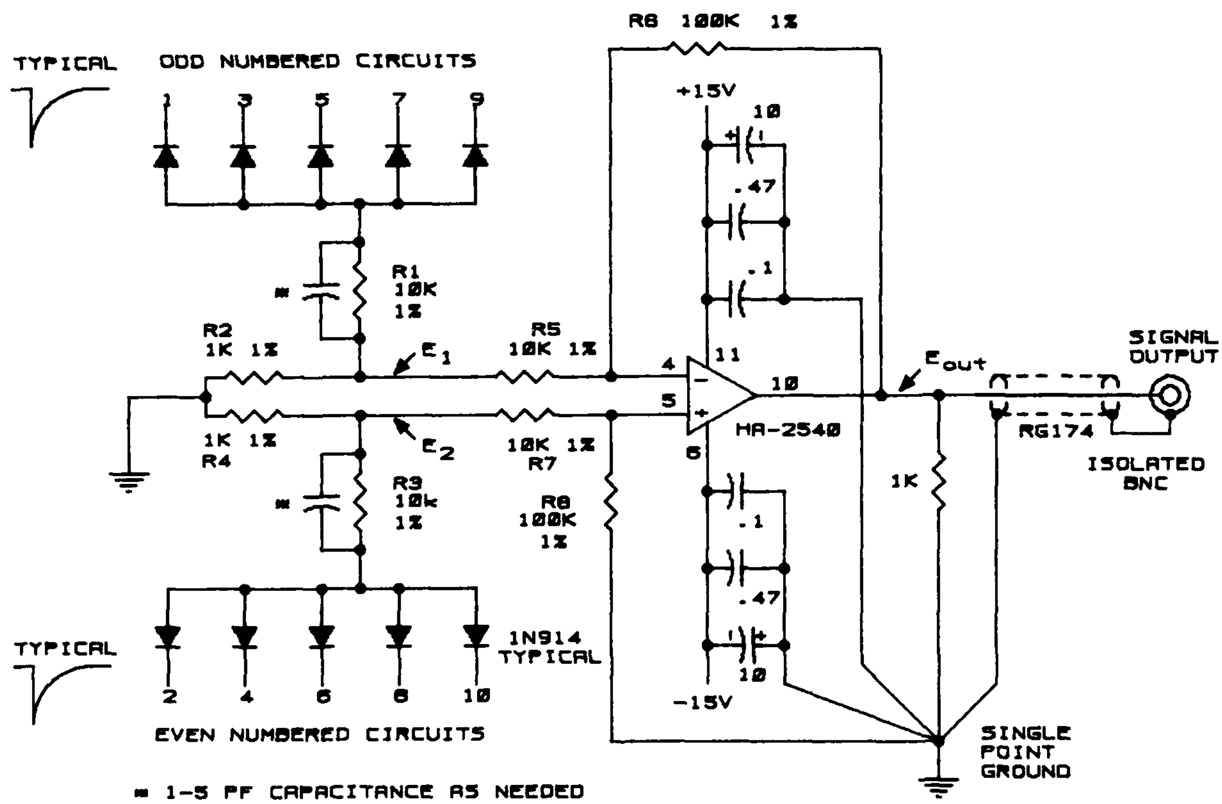


FIGURE 3-3. OUTPUT MIXER AMPLIFIER

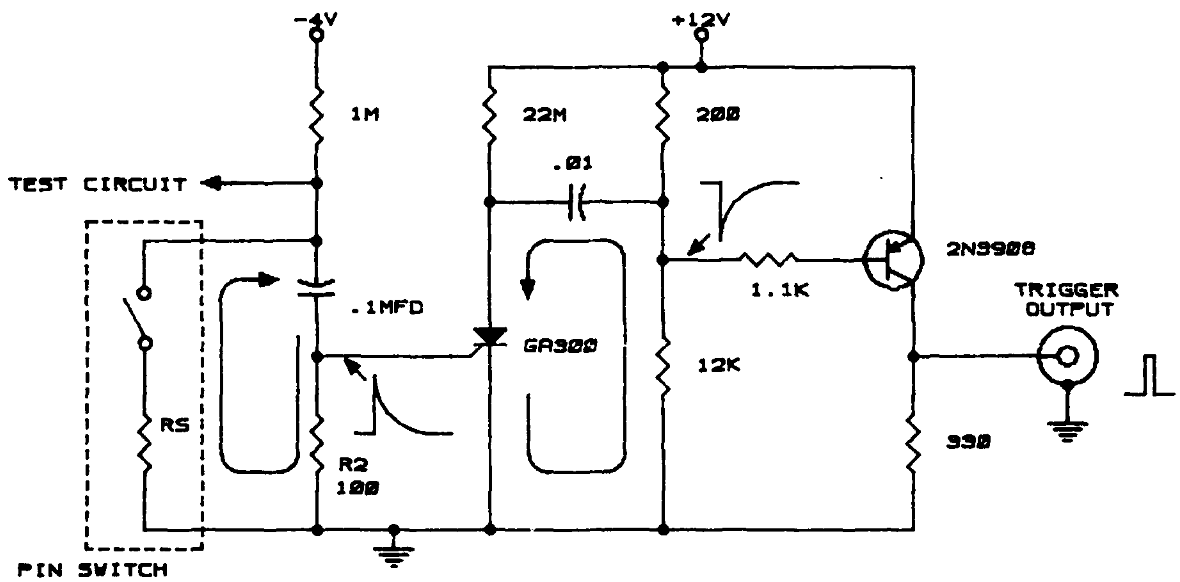


FIGURE 3-4. TRIGGER PIN SWITCH CIRCUIT

probe would be put at some location in the experimental model where its triggering just before the main event is assured in order that all 10 signals could be captured.

As can be seen in Figure 3-4, the circuit uses the typical pin switch components to trigger an SCR like in the other 10 circuits. However, in this case, discharge of the SCR capacitor is used to turn on a 2N3906 switching transistor in order to produce a positive output signal as shown in Figure 1-4. The 200 ohm and the 12k ohm resistors set the bias on the transistor so that it is turned off during standby. The 200 ohm resistor and the .01 MFD capacitor control the width of the output pulse. Lower capacitance will shorten the output pulse duration; more will increase it. When the SCR is triggered, C2 discharges through the SCR to create a negative going signal at the base of the 2N3906 transistor, turning it on. When the current through the SCR drops below its holding value, it turns off and the circuit recharges to the standby conditions. The output pulse width using these components is about 5 microseconds.

Power requirements for the circuits are +/-15 volts for the op-amp and +12 and -4 volts for the pin switch circuits. Power is derived from the +/-33.5 volts dc supply provided in the TM500 mainframe. Tektronix states that the range in variation of their +/-33.5 volts can be from a low of +/-23.7 to a high of +/-40. The 15 volt regulators used for this circuit have an input range of +/-17.5 to +/-30 volts so a preregulator is used to protect them from the possible 40 volt excursion from the mainframe.

In the power supply schematic in Figure 3-5, the A & B lettered and numbered terminals indicate the connections to the Tektronix TM500 mainframe input connector. The input voltage is applied through a fuse to a three component preregulator circuit consisting of a 1k resistor, a 20 volt zener diode, and a transistor. The transistors are provided as part of the mainframe hardware and are not on the pin switch circuit board. The preregulator drops the voltage from the mainframe to about 20 volts at the input of the two voltage regulator integrated circuits. A 7815 regulator regulates the positive voltage to +15 volts for the op-amp circuit. The +15 volts is then dropped to +12 volts through another zener regulator consisting of the 1N4728 zener diode and the 510 ohm resistor. The 12 volts is sent to the pin switch-SCR circuits and to the TEST circuit board via the Samtec interboard connecting pins S7 trough S10. The negative voltage is regulated by the 7915 regulator to -15 volts for the op-amp circuit. The -15 volts is then divided down to -4 volts by a resistive divider and sent to the pin switch probe circuit capacitors.

Voltage and current readings shown in brackets were taken to show nominal relationships at various points in the circuit. At the voltage listed, current drawn from the mainframe to the positive input to the board was 66.84 milliamps at standby and 167.36 ma when the TEST system relays were on. The 100 additional milliamps of current was drawn by the TEST system relays and the 12 volt reading of 11.92 fell to 11.35 when the relays were on. Negative current drawn from the mainframe was -39.19 ma.

A test of the positive voltage regulator was run using a variable dc power supply as the input to the pin switch board. Input voltage was varied from 22 to 40 volts. Output of the preregulator varied slightly about the 19 volt level. The output of the 7815 regulator remained steady at the 14.87 volt level, therefore the onboard regulator system will work over the range

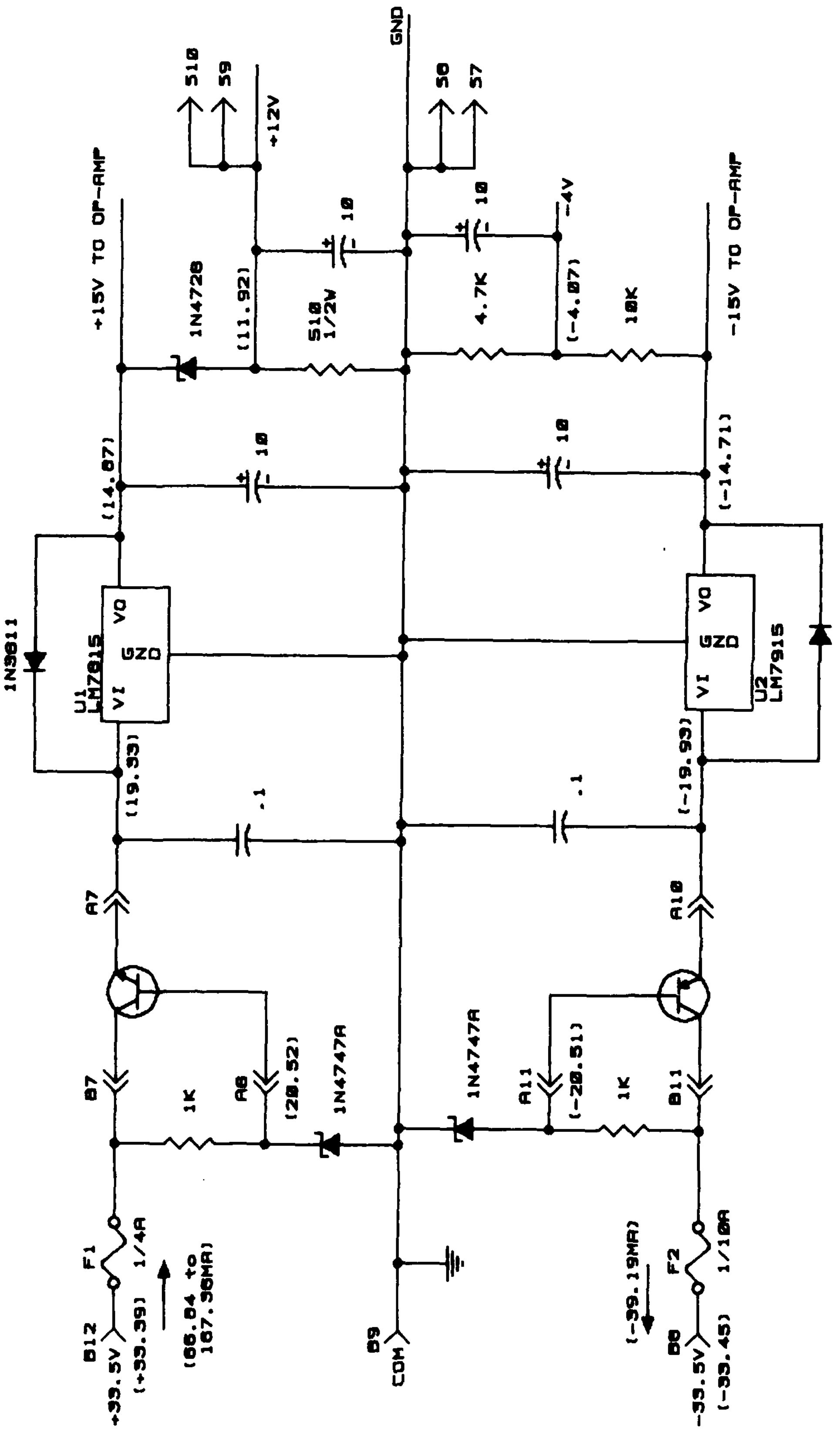


FIGURE 3-5. POWER SUPPLY SCHEMATIC

listed by Tektronix for the excursions of their +/-33.5 volt supply.

All of the circuits described thus far are located on one printed circuit board. The complete board schematic is shown in Figure 3-6. This board is dimensioned to fit the Tektronix single-width plug-in module for the TM500 mainframes and is designed to plug into the mainframe input connector. This board could also stand alone as a pin switch circuit board but would not have any self test capabilities.

In order to test the performance of the PIN SWITCH CIRCUITS instrument and to generate displays such as shown in Figure 1-3, it is necessary for the TEST system to duplicate the switch closure action provided by the pin switch probe. Figure 3-7 shows how the TEST circuit uses a SCR with its anode grounded as a controlled switch to discharge capacitor C1 to simulate probe switch closure. During normal operating conditions, the TEST circuit is isolated from the pin switch circuits by open relay contacts as shown. When a performance test is being run, the relay contacts connect the test SCRs in parallel with the pin probe connections. The positive going edge of a test signal is capacitor coupled to the gate lead of the test SCR to trigger it into conduction. Pin switch capacitor C1 discharges through SCR2 around the loop shown, triggering the pin switch SCR1 as before. When the current through SCR2 falls below its minimum holding value, SCR2 turns off and C1 can recharge back to its supply potential so that, after sufficient recharge time, about 0.3 second, test triggering can be repeated.

Because the pin probe circuit is equivalent to an open circuit as mentioned earlier, the TEST system can discharge capacitor C1 whether or not the probe or cable is connected to the instrument. If the probe or its connecting cable is short circuited, capacitor C1 will lose its charge and no signal can be generated by the TEST circuit, thus, only shorts (or a leakage resistance under 470k ohms) in the system can be detected.

Figure 3-8 shows the complete schematic for the TEST section with the test SCRs and relay contacts in the upper right hand corner. The 4000 series CMOS family of integrated circuits is used for the logic system. The 12 volts applied to the board is used unattenuated for the two relays and is divided down to a nominal 5 volt level for the integrated circuits. The basic operation of the TEST system is to first turn on the relays to connect the TEST system to the pin switch circuits, wait for the relays to pull-in and contact bounce to subside, and then trigger the TEST SCRs. When instrument power is turned on, the TEST system is set to the off state. The very first time any one of the 11 TEST keyboard switches is pressed, the two relays are turned on and they will remain on until turned off by using the END test switch. It must be noted that the act of connecting the TEST circuits to the pin switch board by relay contacts causes transient triggering of the pin switch circuits generating an unuseable display on the oscilloscope. Once the relays are on and circuit bias conditions have readjusted themselves, subsequent and repeated pressing of any of the 11 TEST switches will reliably trigger the pin switch circuits to generate signal output displays. Repeated cycling of the TEST switches is limited by the recharge time of the pin switch capacitors which is about 0.3 second. Too rapid cycling of the TEST switches will produce signal display patterns with reduced amplitude or drop outs. When all performance testing is finished, the TEST system must be turned off by pressing the END TEST switch in order to get a positive READY status indication.

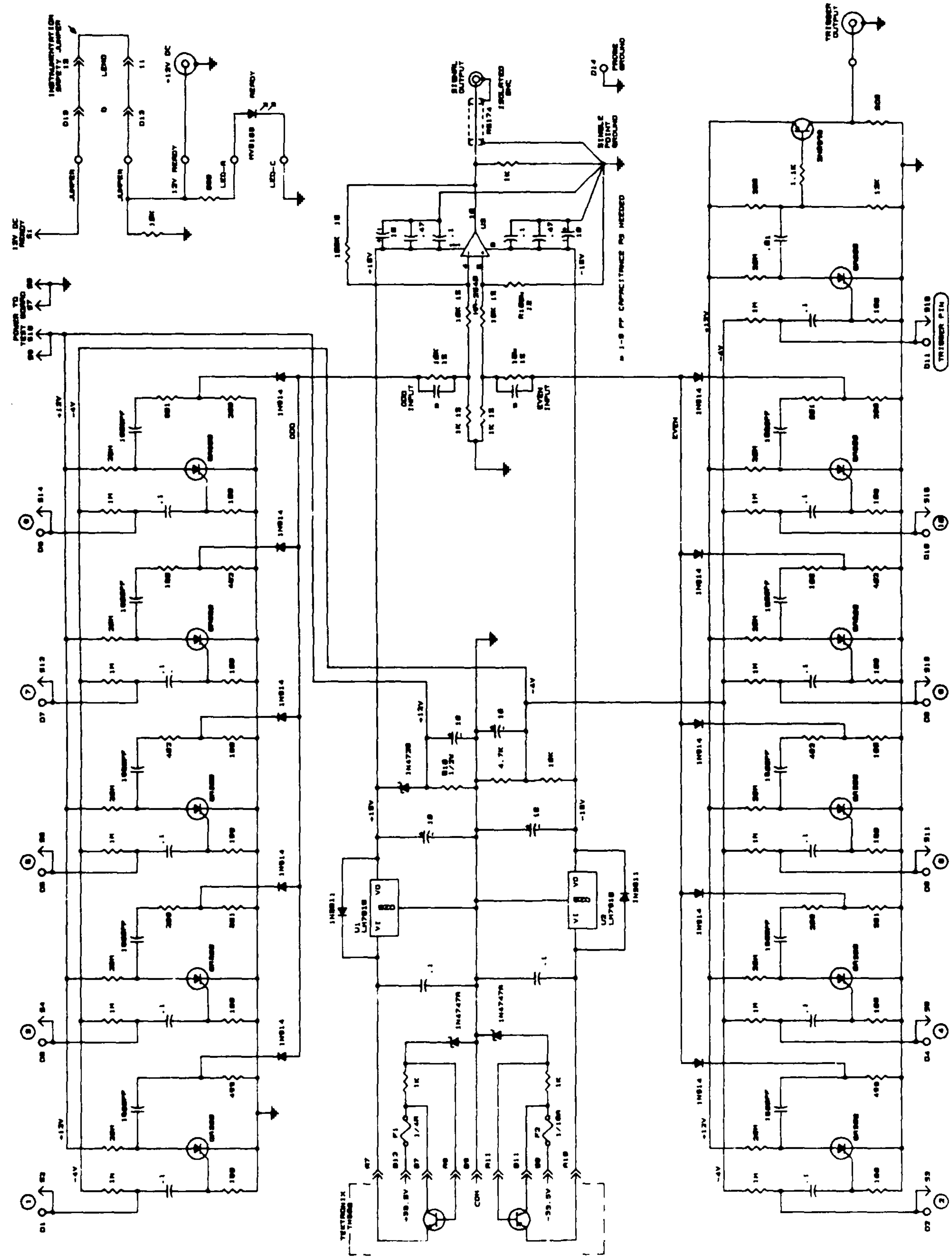


FIGURE 3-6. PIN SWITCH CIRCUIT BOARD SCHEMATIC

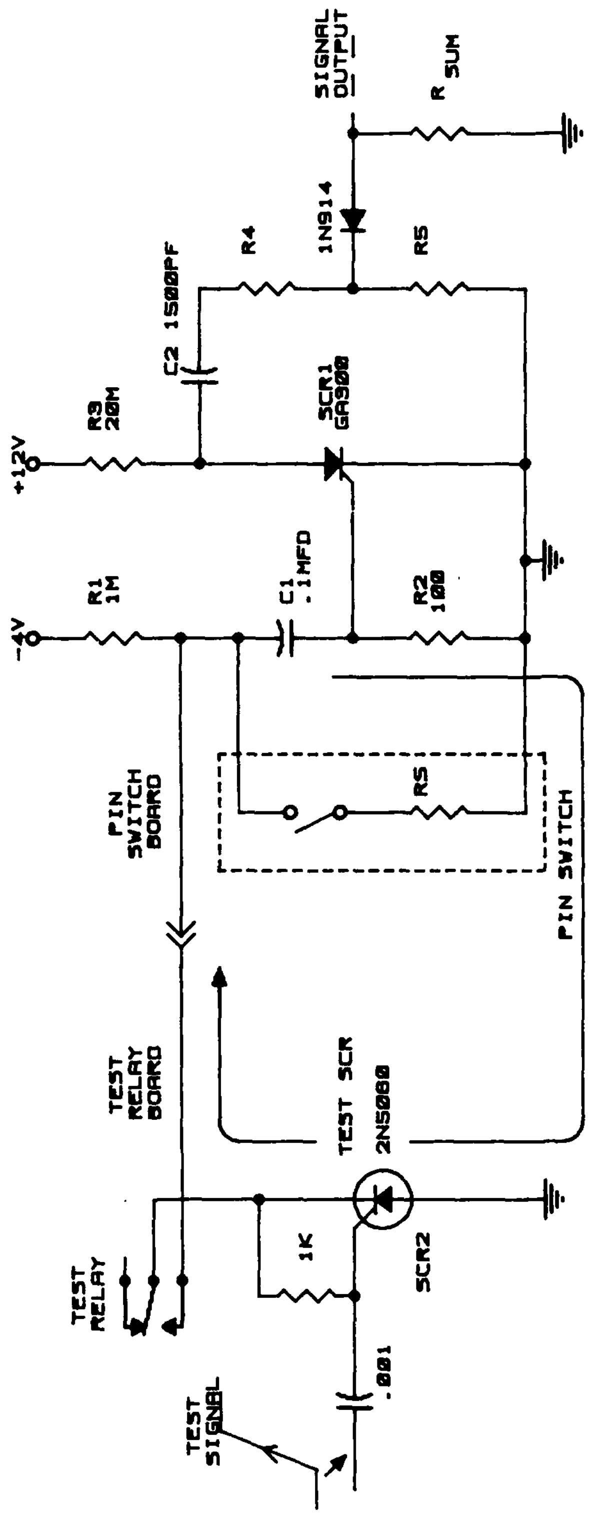


FIGURE 3-7. TEST SCR TRIGGER CIRCUIT

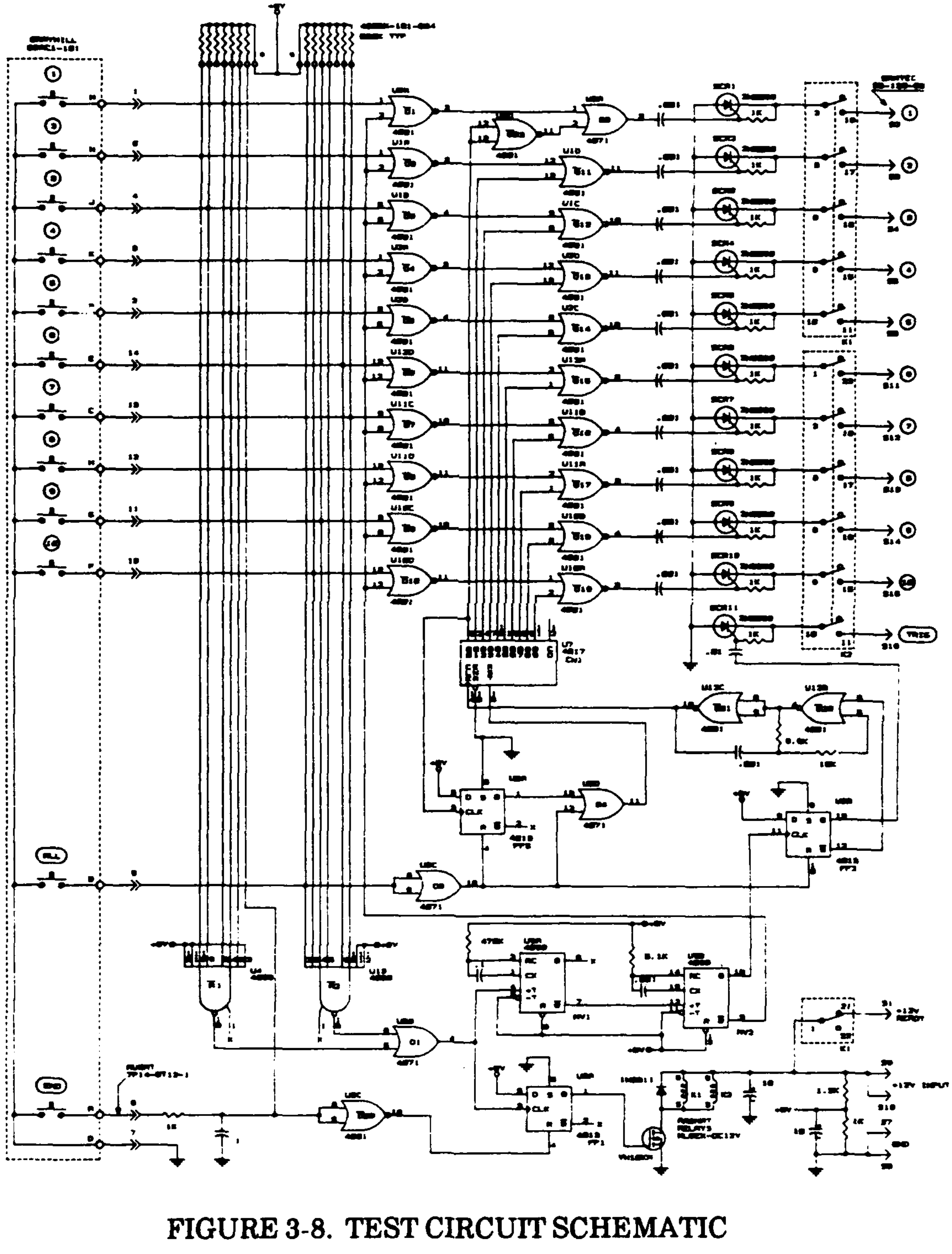


FIGURE 3-8. TEST CIRCUIT SCHEMATIC

Test signals may be generated in either of two ways. Individual signals may be displayed or all ten signals may be generated at one time in a controlled sequence. The first mode of operation to be described is for the generation of individual probe signals one at a time by pressing the selected probe circuit number.

Each of the ten numbered keyboard switches is connected to its own 2-input NOR gate and all 10 switches are connected in parallel to either of two 8-input NAND gates $\overline{A1}$ and $\overline{A2}$. The two NAND gates are operated in parallel so that their outputs combine in OR gate O1 to produce an output in response to the activation of any of the numbered TEST switches. It is the signal from OR gate O1 that is used to turn on the relays and to generate the test SCR trigger pulse. The 2-input NOR gates $\overline{O1}$ through $\overline{O10}$ are used to steer the SCR trigger pulse to the specific SCR selected by the activated TEST switch. In following the typical operating sequence, refer to the schematic in Figure 3-8 and the timing diagram for single circuit operation in Figure 3-9. To illustrate the sequence of operation, pressing TEST switch number 1 grounds inputs to its NOR gate $\overline{O1}$ and to NAND gate $\overline{A1}$, pulling them down to a logic LOW as illustrated in the timing diagram in Figure 3-9. The LOW on $\overline{O1}$ enables the gate and will allow its output to change state in response to a signal to follow on the other input. The same LOW impressed on $\overline{A1}$ causes its output to go HIGH. The HIGH output transition passes through O1 and does two things. First, the HIGH transition from O1 edge triggers FLIP-FLOP FF1 causing its outputs to change logic states. When Q of FF1 (FF1Q) goes to a HIGH level, it turns on relays K1 and K2 via the VN10KM transistor thereby connecting the TEST system to the pin switch board. Once FF1 is triggered, the relays will remain on until a RESET signal is applied to FF1 by the END TEST keyboard switch. As the HIGH transition from O1 triggers FF1, it also triggers MULTIVIBRATOR MV1, the time delay multivibrator. Upon triggering, MV1 changes its output logic states for the duration determined by its RC time constant. This time interval is used to delay triggering of the test SCR until after the relays pull in and contact bounce has subsided. A time delay of about 16 milliseconds is used. When the MV1$\overline{Q}$ output reverts back to HIGH at the end of the time delay, the HIGH transition edge triggers MV2, the test SCR trigger pulse generator. The $\overline{Q}$ output of MV2 is a negative going 5 microsecond wide pulse sent as a common signal to each of the 10 switch input NOR gates $\overline{O1}$ to $\overline{O10}$. The $\overline{Q}$ pulse signal will pass through only the NOR gate that is enabled by the depressed TEST switch, in this example, $\overline{O1}$. Up to this point, where the $\overline{Q}$ SCR trigger pulse passes through the TEST switch input NOR gate, the operation of all 10 numbered TEST switches is exactly the same. In the case of circuit number 1, the trigger signal from $\overline{O1}$ is then passed through an OR gate (O2) to the SCR, while in circuits 2 through 10, the trigger signal is passed through NOR gates ($\overline{O11}$ to $\overline{O19}$) to the SCRs. In every case it is the positive going transition of the signal applied to the SCR gate lead capacitor that triggers the SCR. Subsequent pressing of any numbered TEST switch will repeat the above procedure cycle with the exception that the relays would already be turned on.

The ALL TEST switch is used to generate the controlled triggering of all 10 pin switch circuits in succession from 1 to 10 about 18 microsecond apart to produce the display shown in Figure 1-3. To follow the operation of the ALL TEST switch, refer to the schematic in Figure 3-8 and to the ALL timing diagram in Figure 3-10. Assume that the TEST system is off and that the ALL TEST switch is the first switch pressed. When the ALL switch is pressed, the logic LOW impressed on OR gate O3 passes through as a LOW to enable FF2, FF3, and the DECADE COUNTER CN1 via OR gate O4. The All switch also impresses the

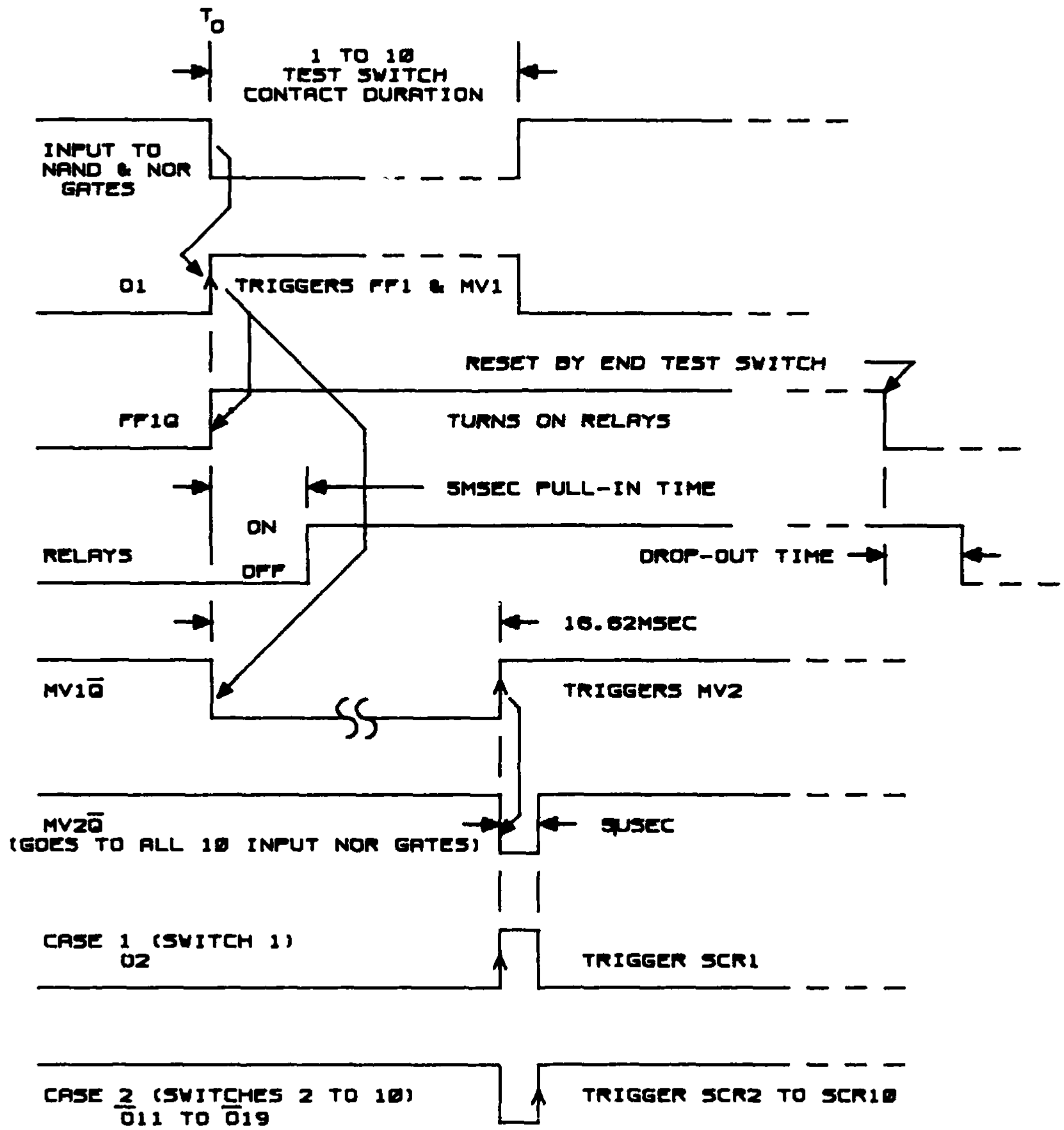


FIGURE 3-9. TIMING DIAGRAM FOR TESTING INDIVIDUAL PIN SWITCH CIRCUITS

LOW on NAND gate $\overline{A}2$ to cause the triggering of FF1 and MV1 to turn on relays K1 and K2 and start the time delay just like the numbered switches do. At the end of the time delay, MV2 is triggered as before. The $\overline{Q}$ output from MV2 plays no part in this mode of operation. The MV2Q output signal, the positive going counterpart, triggers FF2 on the positive transition causing the outputs of FF2 to change states. The FF2Q output goes HIGH and the positive transition triggers SCR11, the test SCR for the TRIGGER pin switch circuit. This generates the TRIGGER OUTPUT SIGNAL for use at the oscilloscope EXTERNAL TRIGGER INPUT connector. At the same time as the FF2Q output goes high, the FF2$\overline{Q}$ output goes LOW and enables NOR gate $\overline{0}20$. NOR gates $\overline{0}20$ and $\overline{0}21$ form a gated oscillator that is controlled by the logic level imposed on pin 6 of $\overline{0}20$ by FF2$\overline{Q}$. A LOW level turns on the oscillator to supply clock pulses to the DECADE COUNTER CN1. Initially, the oscillator output is at a logic HIGH as shown in the timing diagram in Figure 3-10. When the oscillator is turned on by FF2$\overline{Q}$, counter CN1 will increment one count on each positive going transition of the oscillator output signal. Output signals from the DECADE COUNTER, at intervals controlled by the oscillator frequency, are sent to trigger the ten TEST SCRs in sequence. Operation of the DECADE COUNTER sequencing can be followed by referring to the timing diagram. At the first positive going clock transition, the counter increments and outputs Q0 goes LOW and Q1 goes HIGH. The LOW transition from Q0 is inverted to a HIGH by NOR gate $\overline{0}22$ and passes through 02 to trigger SCR1. On the second positive going clock pulse transition, the counter increments and Q1 goes back to LOW and Q2 goes HIGH. When Q1 goes LOW, the transition is inverted to a positive one by NOR gate $\overline{0}11$ to trigger SCR2. The third positive clock transition takes Q2 back to LOW and Q3 goes HIGH. The LOW transition of Q2, inverted by 012 triggers SCR3. The sequence shown in Figure 3-10 ripples through the counter with the LOW transition of each output, inverted by the NOR gates, triggering the SCRs in sequence. On the 10th clock pulse, Q9 goes LOW to trigger SCR10 and Q0 goes back to HIGH to complete one cycle of decade counting. The HIGH transition from Q0 triggers FF3, causing its Q output to go to a HIGH level state. The HIGH level is passed through OR gate 04 to the RESET control pin on the counter to disable it and stop the counting. Thus the DECADE COUNTER counts exactly 10 clock pulses, triggering a SCR on each count, and stops after one cycle even though the gated oscillator is still running. All test signal generation occurs in less than 20 msec after the ALL TEST switch is pressed. When the ALL TEST switch is released (by the operator removing his finger from the button), OR gate 03 goes back to a HIGH output to reset FF2, FF3, and the DECADE COUNTER. When FF2 resets, its outputs revert back to their initial states and the HIGH from $\overline{Q}$ turns off the gated oscillator. When FF3 resets, its Q output goes back to LOW but the HIGH from gate 03 passes through 04 to continue to hold the counter off and reset to a count of zero. Subsequent pressing of the ALL TEST switch at this time would repeat the cycle described, with the exception that once again the relays would already be turned on.

Once the TEST system relays are turned on, the TEST switches may be pressed in any order desired. When all performance testing is completed, pressing the END TEST switch discharges the 1 MFD capacitor on the input of NOR gate $\overline{0}23$ through a 1k resistor to ground. With the input pulled LOW, the output of $\overline{0}23$ goes HIGH to reset FF1. When FF1 resets, its Q output goes back to LOW, turning off the VN10KM transistor and the two relays. The TEST circuit is then turned off, reset to its standby condition, and disconnected from the pin switch circuit board.

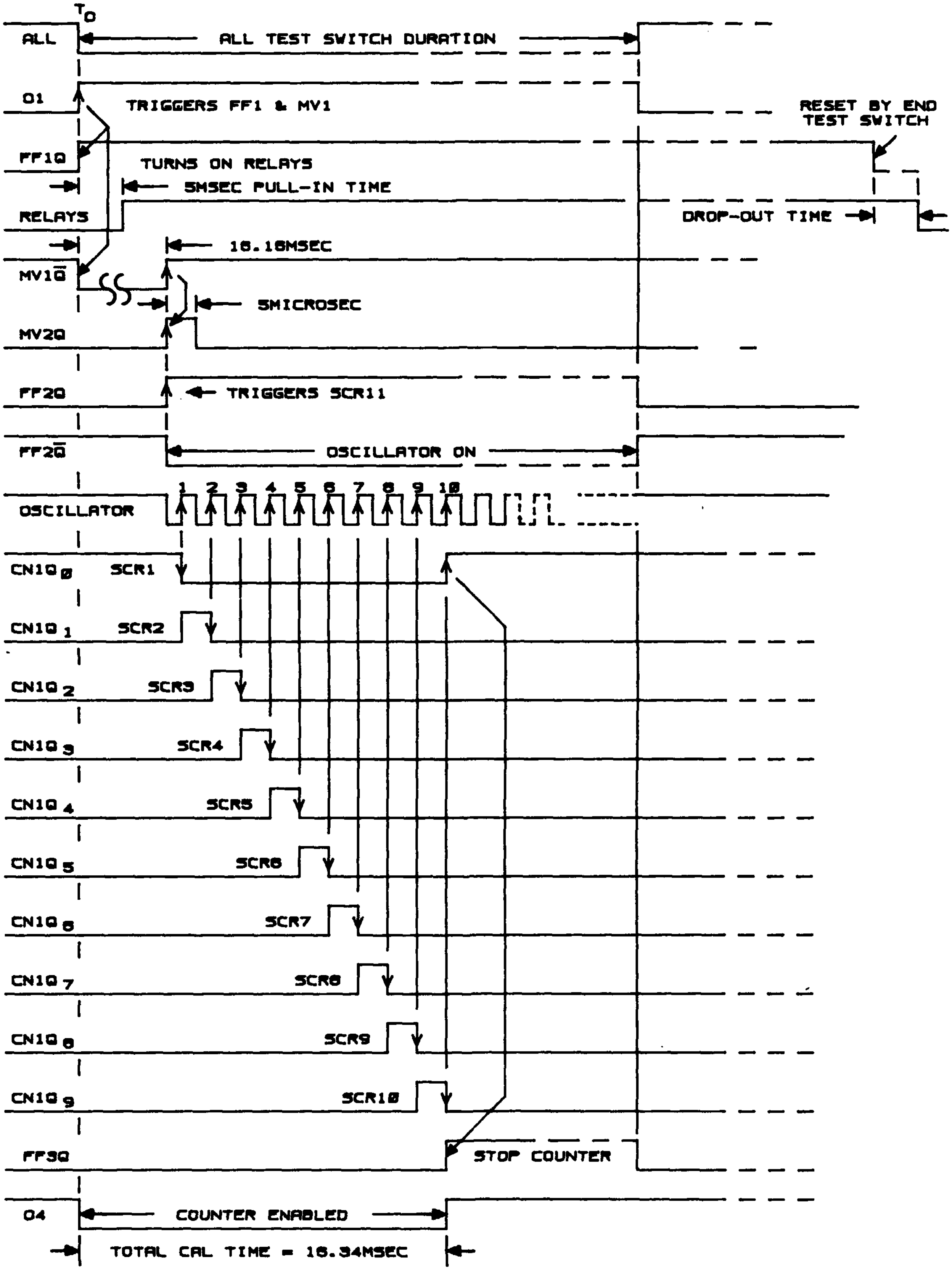


FIGURE 3-10. TIMING DIGRAM FOR TESTING ALL 11 CIRCUITS

Because the FLIP-FLOPS and the DECADE COUNTER are edge triggered devices, the are susceptible to transient triggering into false logic states when first turning on instrument power. The normal HIGH output state assumed by OR gate 03 as the power supply voltage comes up is used to force FF2 and FF3 to their proper initial logic states, to set the DECADE COUNTER to an initial count of zero, and to disable all three devices. The END TEST switch NOR gate $\overline{0}$23 used to reset FF1 after it is triggered is also made to force FF1 to its proper logic state as power comes up by the network on its input. This power up circuit is shown in Figure 3-11. When power is turned on, the 1MFD capacitor on the input of $\overline{0}$23 momentarily acts as a short circuit, impressing a LOW on the gate and causing its output to go HIGH. The HIGH impressed on the RESET pin of FF1 forces the outputs to their required initial logic states. The output of $\overline{0}$23 remains at the HIGH level as the 1MFD capacitor charges to the supply potential through the 560k pull-up resistor. When the capacitor charges to the logic HIGH input level threshold of the gate, the gate's output goes LOW. The LOW state is the normal standby level and allows FF1 to be triggerable. With the resistor and capacitor used, the output of $\overline{0}$23 goes HIGH for about 460 msec when power is turned on to cover any transients generated as the supply rises to 15 volts.

The READY circuit shown in Figure 3-12 is used to indicate that the pin switch probe assembly cable is attached to the instrument and that the TEST circuit is turned off. When the TEST system is turned off, the +12 volts is passed through a set of normally closed contacts to the probe cable assembly safety jumper installed in the 10 conductor cable connector. If the cable is connected to the instrument, the jumper in the connector completes the circuit and the 12 volts is applied to the light emitting diode (LED) circuit and the monitor connector. The 10k resistor to ground is used to pull down the inputs of the monitor circuit located in the panel in the control room.

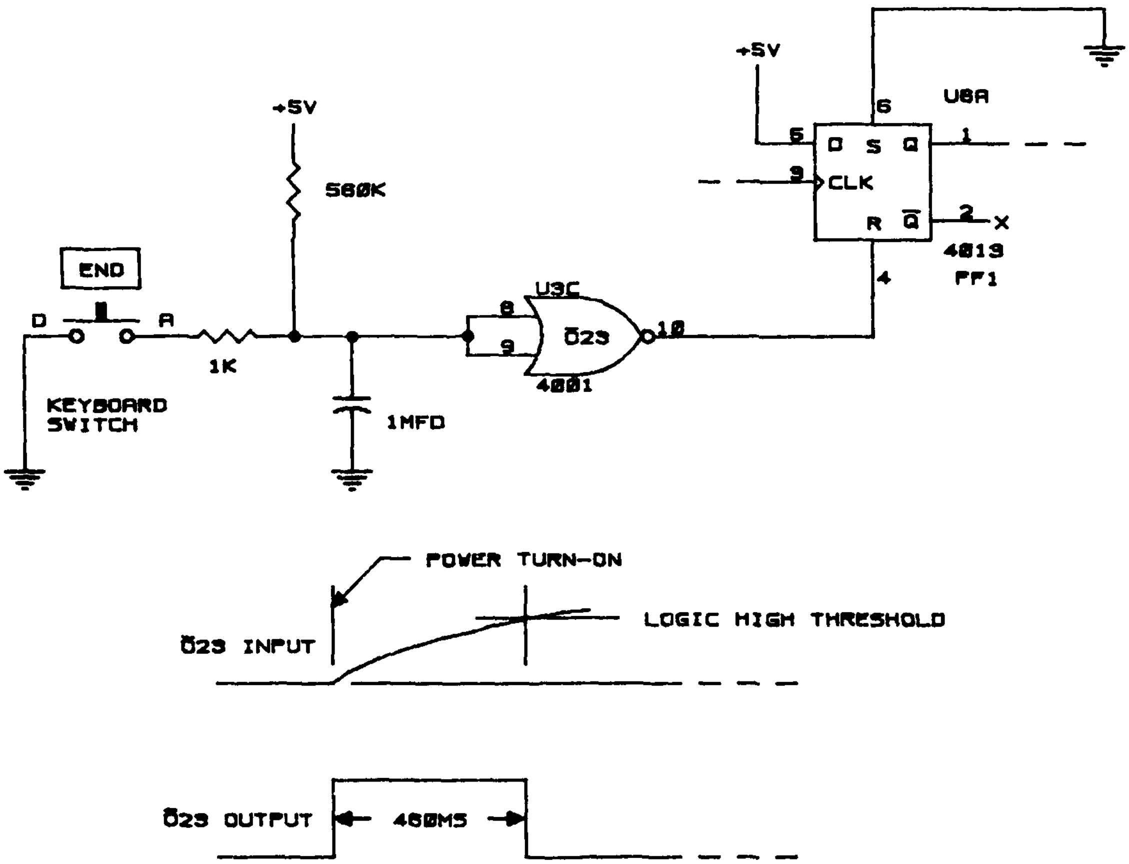


FIGURE 3-11. POWER-UP INITIALIZING - SET FF1

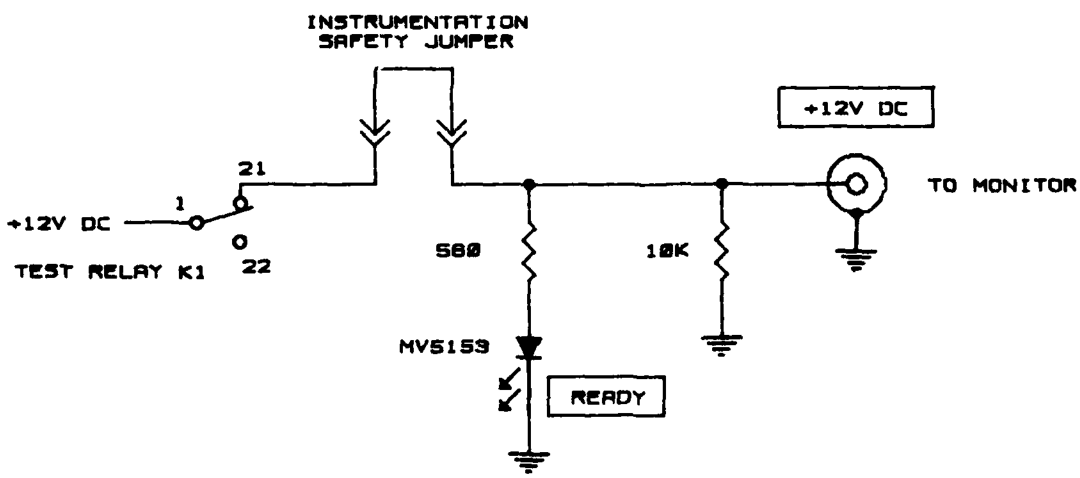


FIGURE 3-12. READY STATUS INDICATOR SYSTEM

CHAPTER 4

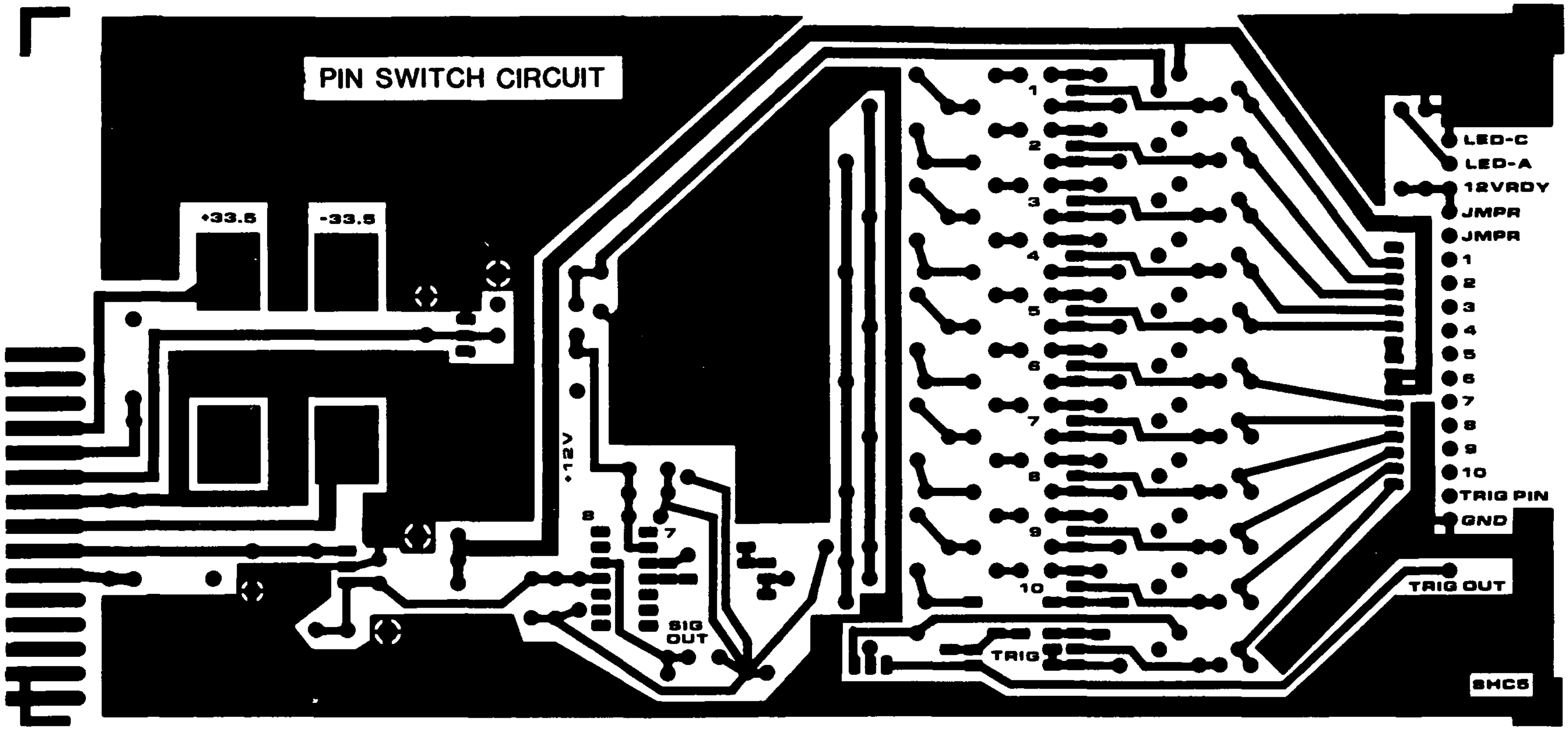
MECHANICAL SPECIFICATIONS

The printed circuit board artwork and manufacturing instructions are shown in Figures 4-1 and 4-2 for the pin switch board, and in Figures 4-3 and 4-4 for the TEST board. Circuit component layouts for the boards are shown in Figures 4-5 and 4-6.

Figure 4-7 shows the Metalphoto artwork for the front panel and lists instructions for cutting and drilling for final assembly. Figure 4-8 is an exploded view diagram showing how to assemble the instrument. Parts for this assembly are listed in Table 4-1. Note that Tektronix requires the use of a POZIDRIVE screwdriver to assemble their component parts from their blank plug-in module 040-0652-05. The 1/4-inch hole for the LED in the front panel must be opened up to 3/8 inch in the subpanels to accept the LED mounting hardware. Before any assembly work is done, the top frame rail must be tapped for the 6-32 screws that are used to hold the front panel to the top frame. To assemble, first insert the grounding spring in the top frame rail and insert the retaining latch and release bar in the bottom rail. Next, connect the two subpanels to the bottom rail using two 6-32 flat head screws. Attach the front panel to the subpanels using the three BNC connectors. Screw the top of the front panel to the top rail with two 6-32 round head screws. Attach the D connector and latching blocks. At this time the pin switch board could be connected to the top and bottom rails for stabilizing the unit. Plug in the LED bezel from the front, snap in the LED and use the retaining ring to hold the LED in place. Next, attach the keyboard switch and secure in place with epoxy if the need arises.

Wiring of the keypad switch is shown in Figure 4-9. Wiring of the pin switch board to the front panel and all the way out to the probes is shown on Figure 4-10. Detailed wiring of the cable assemblies is shown in Figures 4-11 and 4-12. The safety shorting plug used during instrumenting of the explosive charge is shown in Figure 4-13. The complete parts list for the instrument is shown in Table 4-2.

Figure 4-14 shows a test box made to aid in identifying the pin switch circuit number in the ten conductor cable. This was originally built to aid a technician who is color blind but the box has proven to be useful in some troubleshooting applications as well. In use, the probe cable is connected to the box and the technician takes any cable wire and touches the exposed end to the ground return. The corresponding LED lights up to identify the wire being tested and the wire is then tagged with its circuit number. Note that the box works only if the jumper wire is in place in the probe cable connector and that it only draws power when a wire is being tested.



1/16" THICK FIBERGLASS BOARD
1 ØZ. COPPER PLATING
TIN-LEAD PLATED
DOUBLE SIDED, PLATED THROUGH HOLES
GOLD PLATE EDGE CONNECTOR

NØ. 50 DRILL, 8 HOLES FOR FUSECLIPS
NØ. 28 DRILL, 5 HOLES FOR MOUNTING
NO. 65 DRILL, ALL OTHER HOLES
ALL HOLE SIZES ARE AFTER PLATING
SHEAR TO INSIDE OF CORNER MARKS

FIGURE 4-1. PIN SWITCH PRINTED CIRCUIT BOARD ARTWORK - TOP SIDE

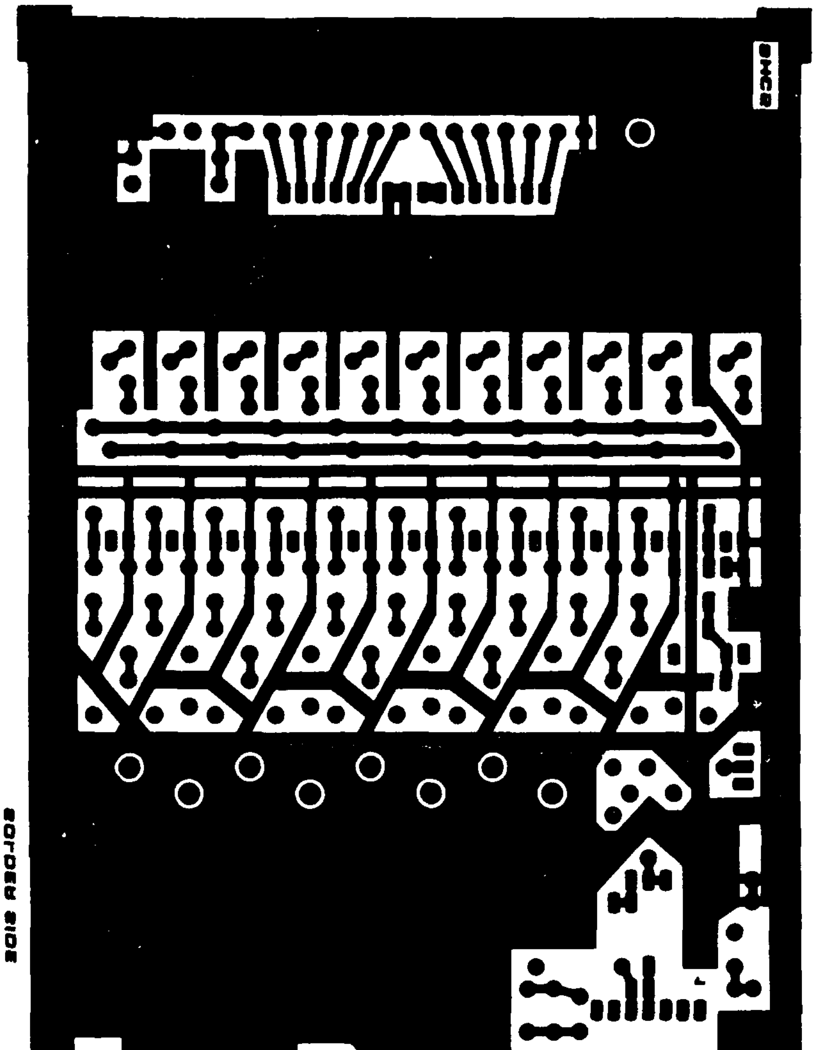
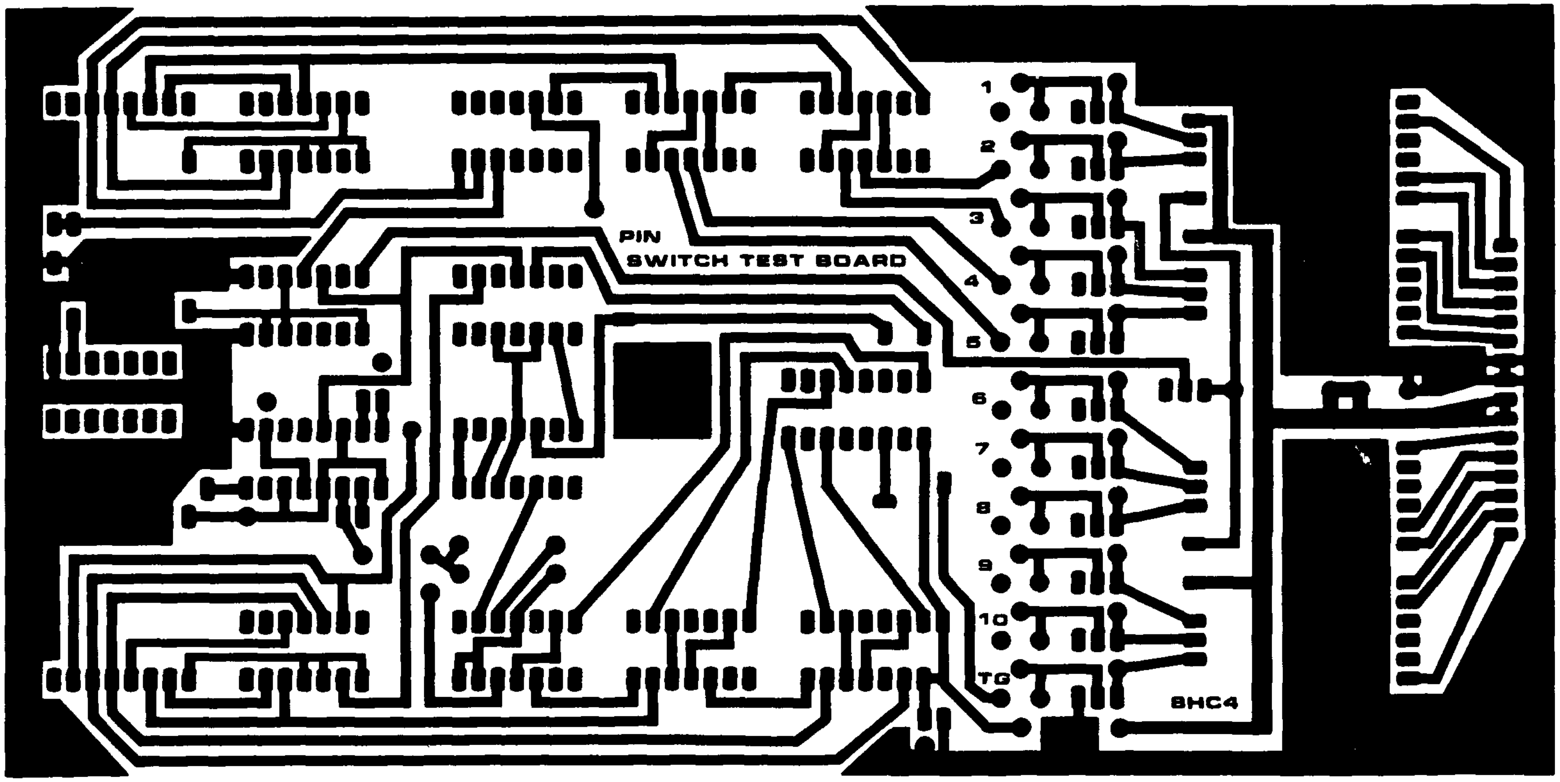


FIGURE 4-2. PIN SWITCH PRINTED CIRCUIT BOARD ARTWORK - BOTTOM



1/16" THICK FIBERGLASS
1 0Z. COPPER PLATING
TIN-LEAD PLATED
DOUBLE SIDED, PLATED THROUGH HOLES
ONE HOLE, CENTERED IN CENTER SQUARE, NO. 28 DRILL (.140) AFTER PLATING
ALL OTHER HOLES, NO. 65 DRILL (.035) AFTER PLATING

FIGURE 4-3. TEST PRINTED CIRCUIT BOARD ARTWORK - TOP SIDE

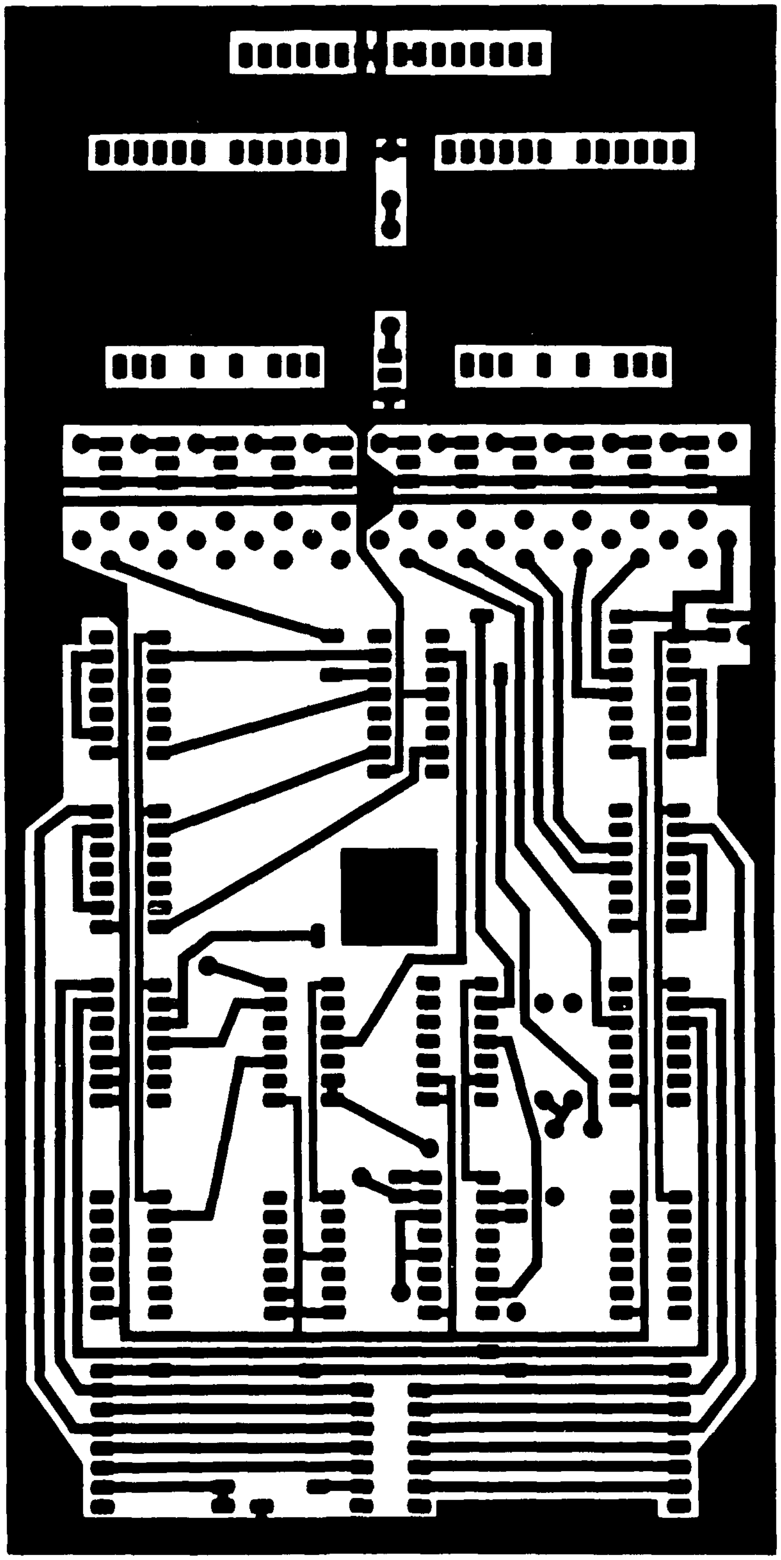
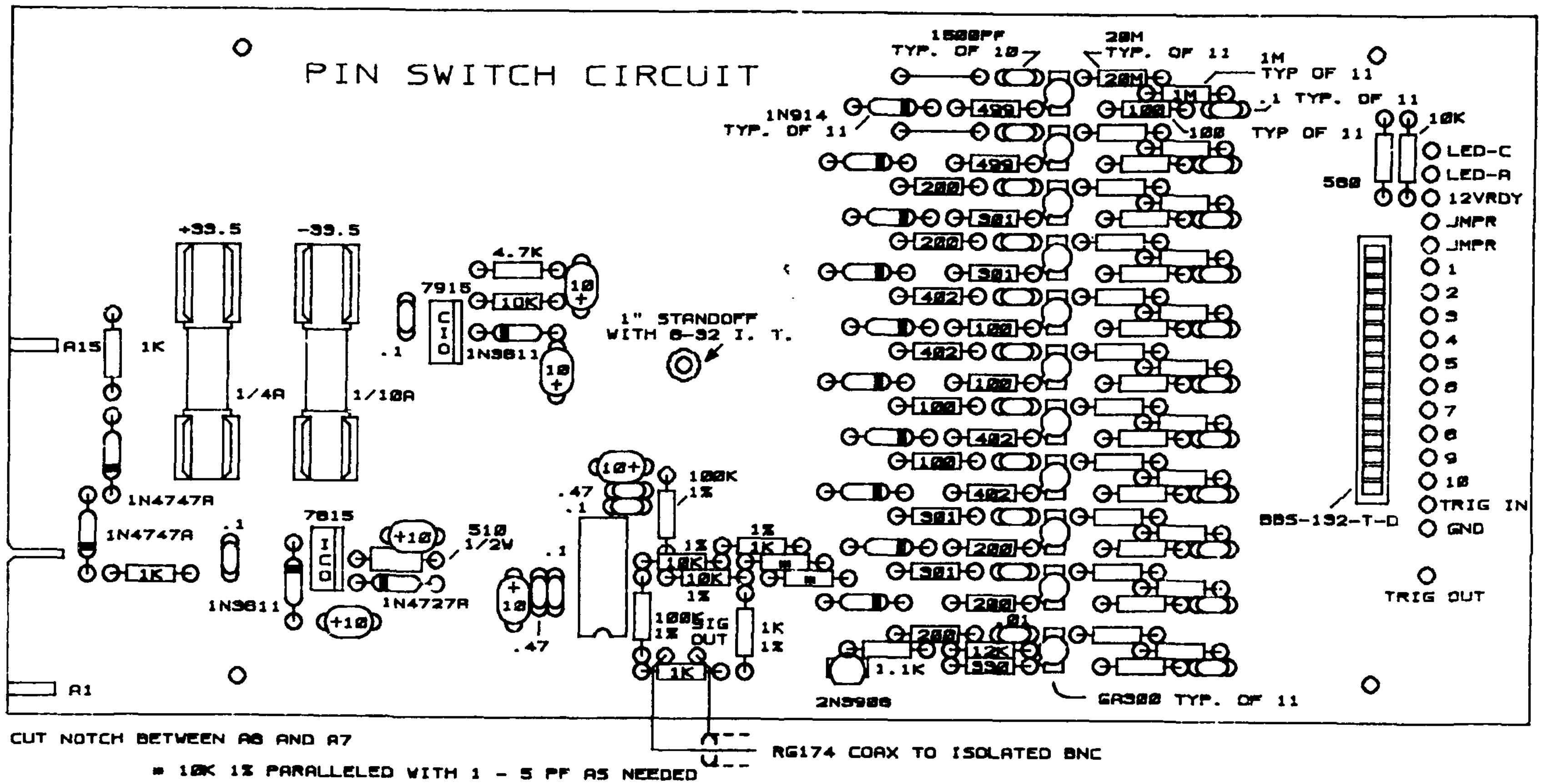


FIGURE 4-4. TEST PRINTED CIRCUIT BOARD ARTWORK - BOTTOM



RESISTORS 1% METAL FILM

4	100
4	200
4	301
4	402
2	499
2	1K
4	10K
2	100K

5% CARBON, 1/2W

1	510

RESISTORS 5% 1/4W

11	100
1	200
1	330
1	560
3	1K
1	1.1K
1	4.7K
2	10K
1	12K
11	1M
11	20M

SOLID STATE

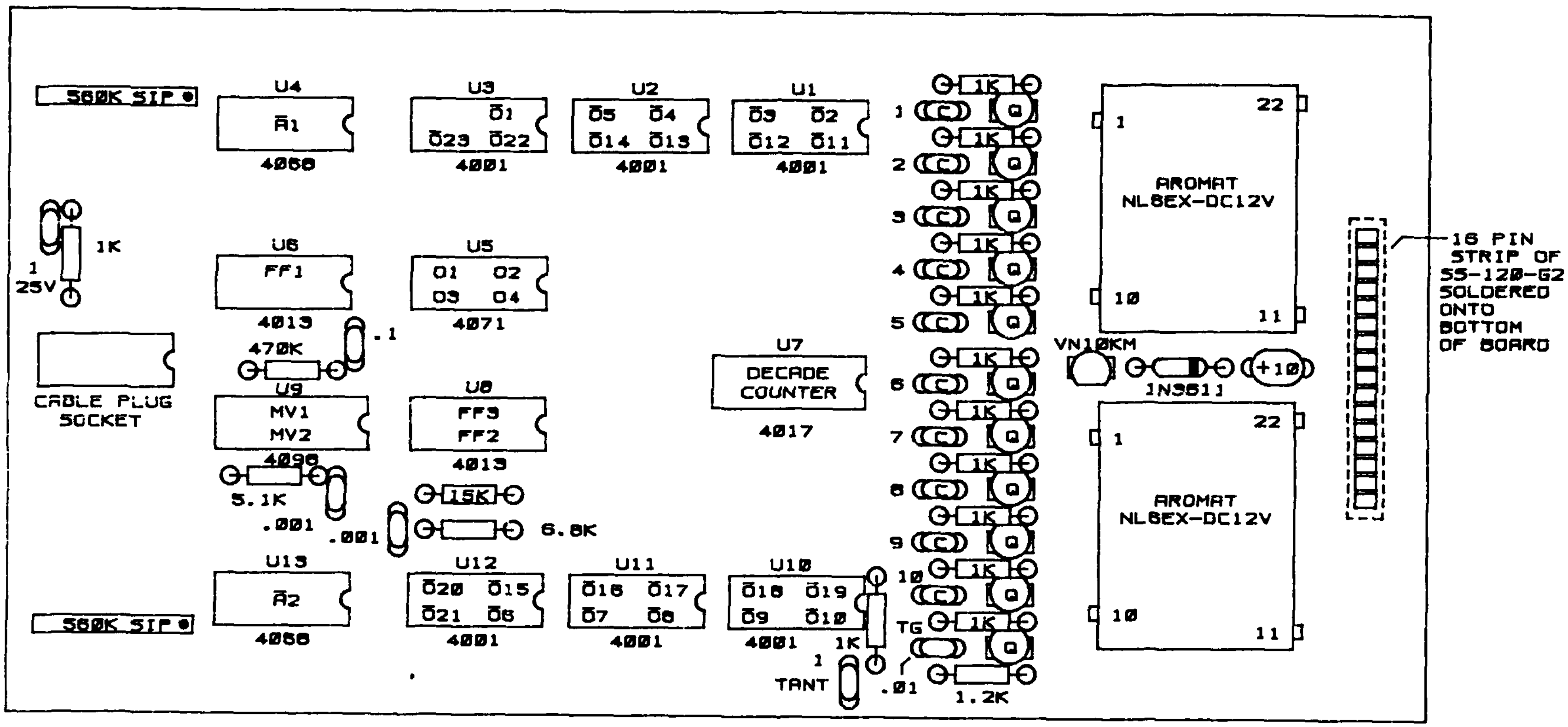
2	1N4747A ZENER DIODE
1	1N4728A ZENER DIODE
2	1N3611 DIODE
10	1N914 DIODE
11	GA300 SCR
1	2N3906 TRANSISTOR
1	7815 POS VOLT REG
1	7915 NEG VOLT REG
1	HA-2540 OPERATIONAL AMPLIFIER

CAPACITORS

10	1500PF
1	.01MFD
14	.1MFD
2	.47MFD
6	10MFD, TANTALUM

4	FUSECLIPS
1	1/10A 3AG FUSE
1	1/4A 3AG FUSE
11	SETS OF 3 EA, SS-120-G2 SOCKET PINS
1	SET OF 16, BBS-132-T-D INTERCONNECT PINS
1	1" METAL STANDOFF WITH 6-32 INTERNAL THREADS
1	6-32 X 1/4 SCREW
1	14 PIN DIP SOCKET

FIGURE 4-5. PIN SWITCH PRINTED CIRCUIT BOARD COMPONENT LAYOUT



6	U1-U3, U10-U12 = 4001	12	C = .001 MFD	13	1K OHM
2	U4, U13 = 4060	1	.01 MFD	1	1.2K
1	U5 = 4071	1	.1 MFD	1	5.1K
2	U6, U8 = 4013	1	1 MFD, CERAMIC	1	6.8K
1	U7 = 4017	1	1 MFD, TANTALUM	1	15K
1	U9 = 4098	1	10 MFD, TANTALUM	1	470K
1	DIODE, 1N5611	2	RELAY, NL6EX-12VDC, AROMAT	2	560K SIP NETWORK
1	TRANSISTOR, VN10KM	12	SETS, OF 3 PINS EACH, 55-120-G2	12	14 PIN DIP SOCKET
11	Q = 2N5060 SCR	1	SET OF 16 PINS, 55-120-G2	2	16 PIN DIP SOCKET

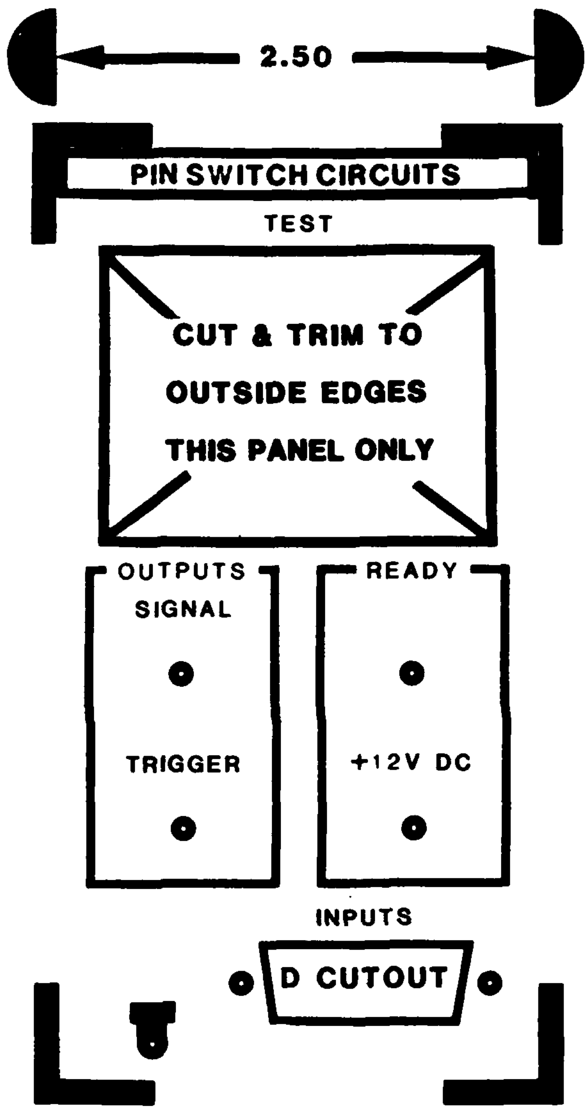
FIGURE 4-6. TEST PRINTED CIRCUIT BOARD COMPONENT LAYOUT

Front panel dimensions are equal to Tektronix part No. 333-1483-03. Align front panel with plastic subpanel, mark and drill through top corners for 6-32 screws to fasten to top frame section.

Rectangular hole for the keyboard switch is cut out of the front panel ONLY. For the plastic subpanel and back panel, drill 4 holes for the switch mounting pins and cut out slots for the terminal pins. Switch can be secured in place by epoxy at four corner pins as last act of assembly.

The D connector hole is cut out through all three panels. The BNC connector holes are drilled through all three panels. The SIGNAL BNC hole is 1/2" dia. and the other two BNC holes are 3/8" dia. drill. The READY LED hole is 1/4" dia. in the front panel and is opened up to 3/8" dia. in the back two subpanels. The D connector mounting screw holes are No. 33 drill.

Cut out the Tektronix latching/release tab hole in the front panel only.



1/16" aluminum
Black letters on silver background
Shear to inside edges of corner marks

FIGURE 4-7. FRONT PANEL METALPHOTO ARTWORK AND CUT AND DRILL GUIDE

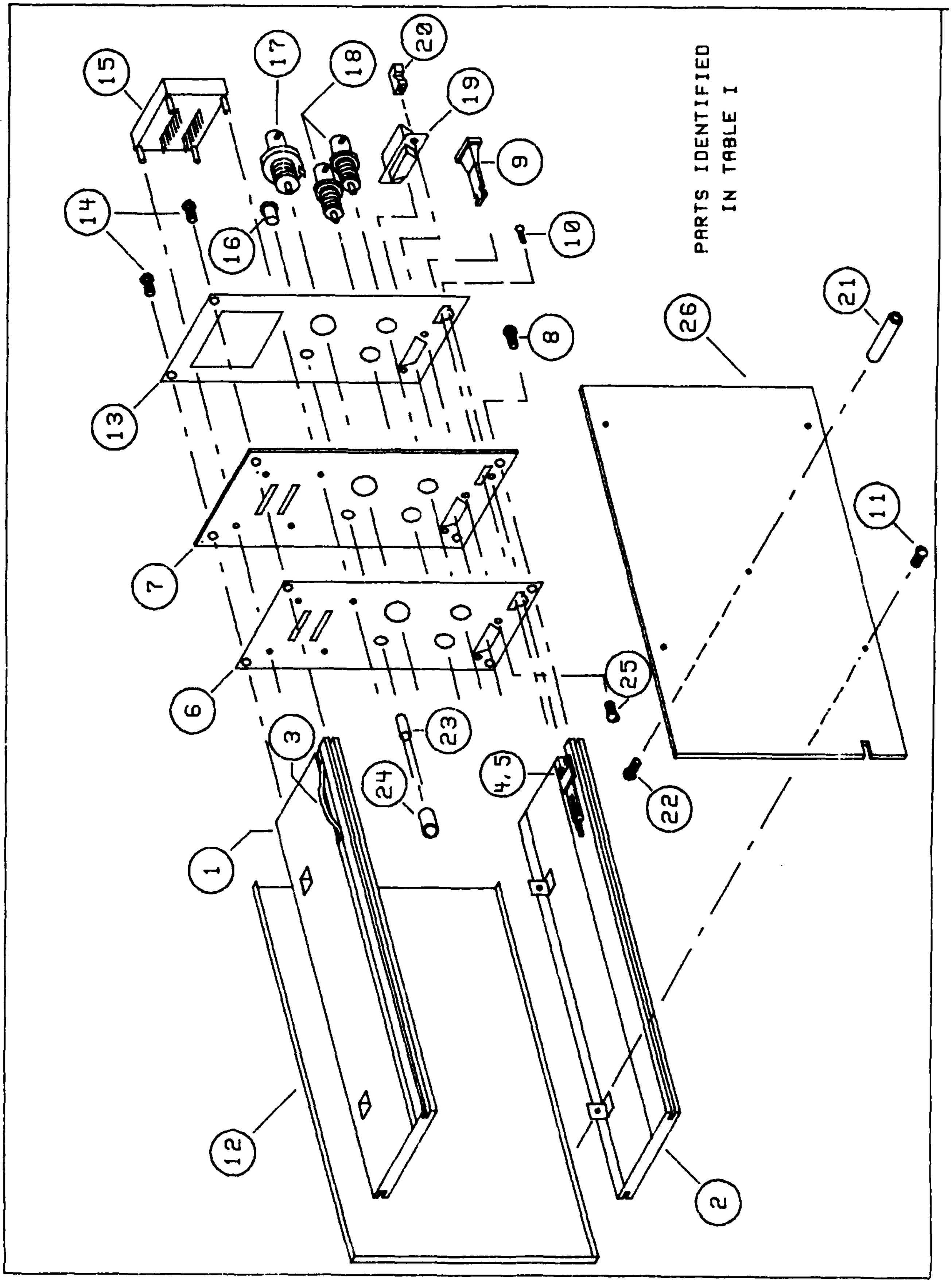


FIGURE 4-8. CHASSIS ASSEMBLY GUIDE

TABLE 4-1. CHASSIS ASSEMBLY PARTS

ITEM	QUANTITY		DESCRIPTION
1	1	426-0725-00	frame section, top
2	1	426-0724-00	frame section, bottom
3	1	214-1061-00	spring, electrical ground
4	1	105-0718-01	release bar
5	1	105-0719-00	retaining latch
6	1	200-1273-02	subpanel, back
7	1	386-2402-05	subpanel, front
8	2	213-0229-00	screw, thread forming. #6-32x.375 FH
9	1	366-2402-05	knob, latch
10	1	213-0254-00	screw. #2-32x.250 FH
11	4	213-0146-00	screw, thread forming, #6-32x.313 PH
12	2	337-1399-00	shield, electrical (side panel)
13	1		front panel
14	2		screw, #6-32x.500 PH
15	1		switch, keyboard, Grayhill 83AC1-101
16	1		bezel, LED
17	1		connector, panel, isolated BNC
18	2		connector, panel, BNC
19	1		connector, 15 pin D, socket
20	2		blocks, latching, TRW SD-LB
21	1		standoff, metal, 1", with #6-32 internal threads
22	1		screw, #6-32x.250 PH
23	1		diode, light emitting, MV5153
24	1		ring, retaining, LED
25	2		screw, #4-40x.375 PH
26	1		printed circuit board, pin switch

Items 1 through 12 are parts furnished in the Tektronix TM500 Blank Plug-in Module kit 040-0652-05. Tektronix states that assembly of their modules require the use of a #2 POZIDRIVE screwdriver; do not use a Phillips.

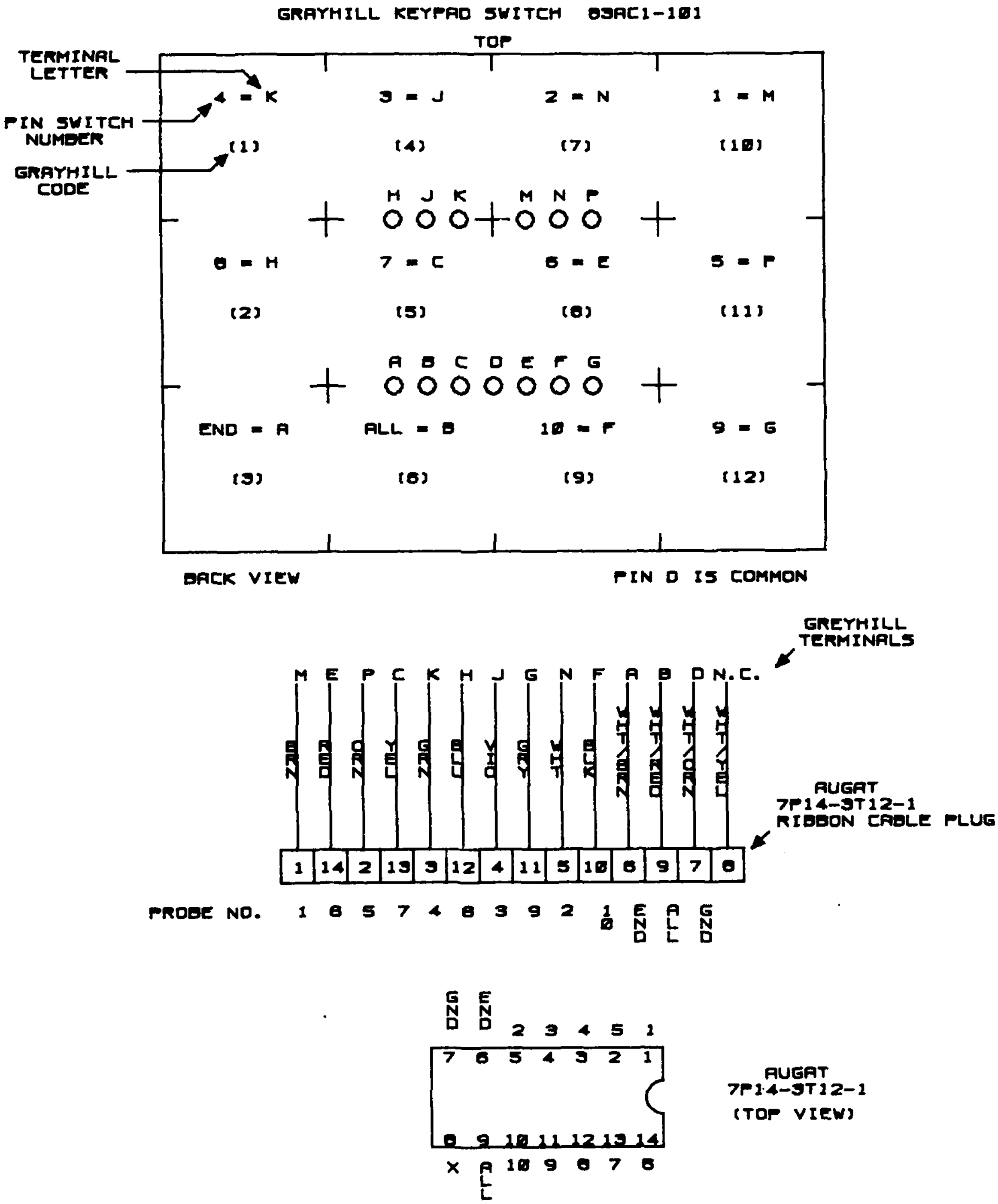


FIGURE 4-9. KEYPAD SWITCH WIRING

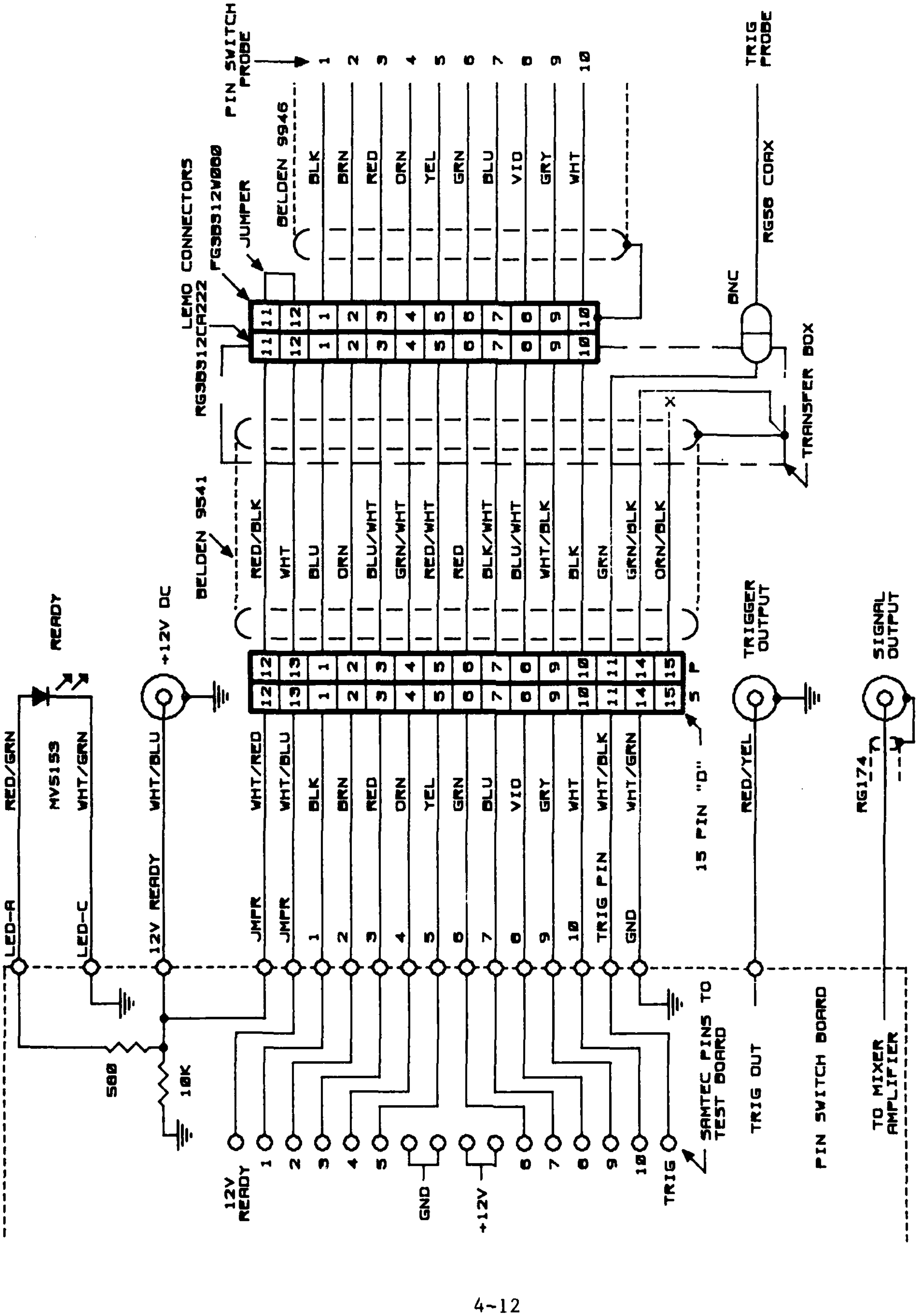


FIGURE 4-10. FRONT PANEL AND CABLE CONNECTOR WIRING AND COLOR CODES

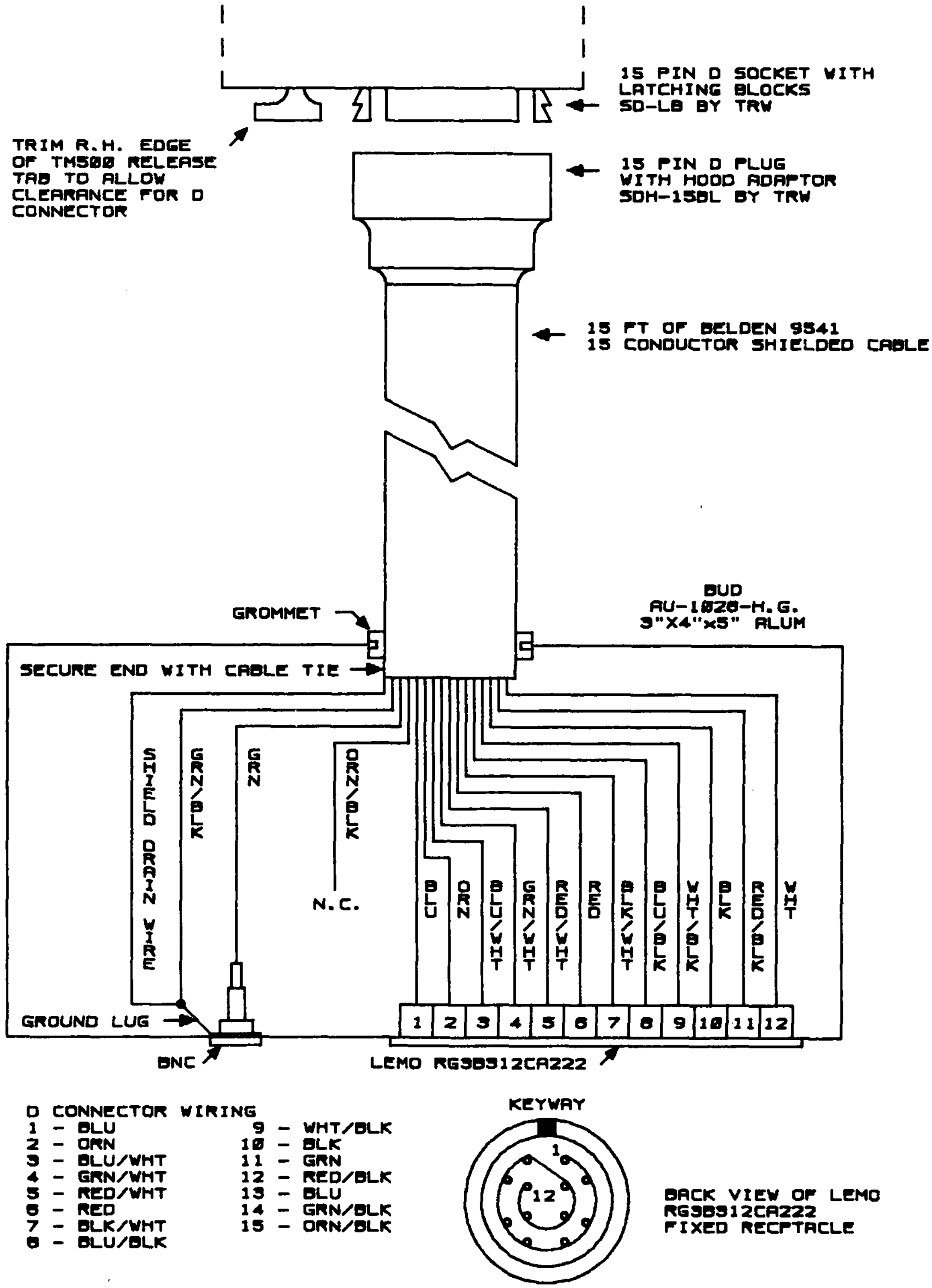
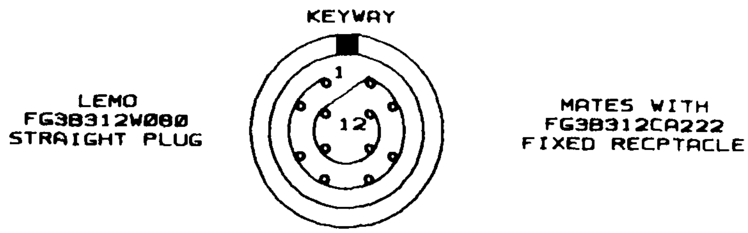
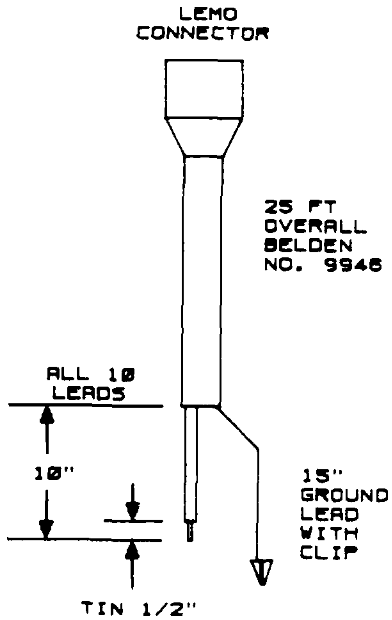


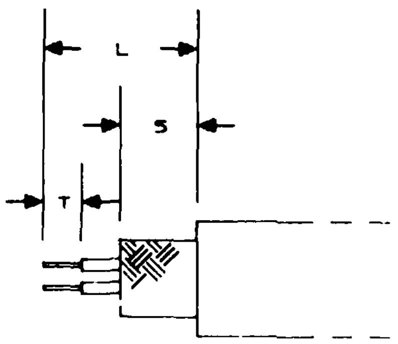
FIGURE 4-11. "D" INSTRUMENT CABLE AND TRANSFER BOX



BACK VIEW OF
CABLE CONNECTOR

PIN SWITCH CIRCUIT NO.	LEMO PIN NO.	10 CONDUCTOR WIRE COLOR
1	1	BLK
2	2	BRN
3	3	RED
4	4	ORN
5	5	YEL
6	6	GRN
7	7	BLU
8	8	VIO
9	9	GRY
10	10	WHT
READY	11	JUMPER
READY	12	JUMPER





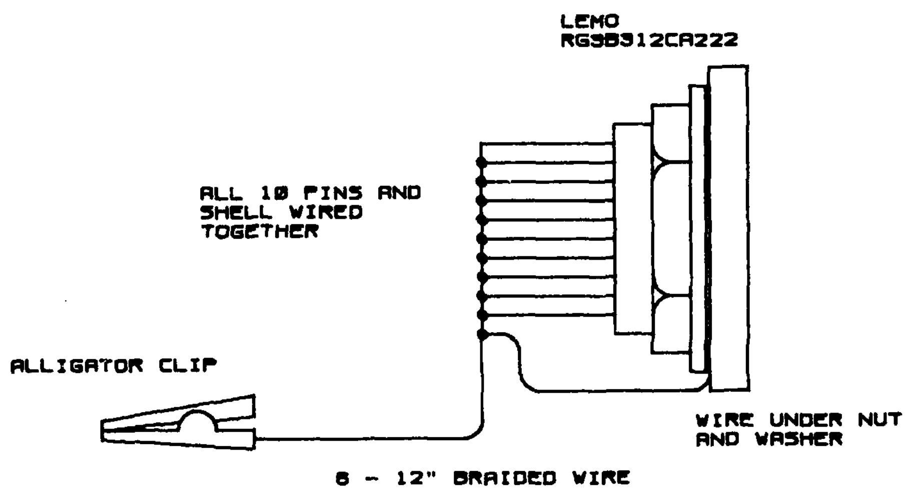
$L = .827\ (21)\ \pm 4\%$

$S = .394\ (10)\ \pm 3\%$

$T = .118\ (3)\ \pm 5\%$

CABLE STRIPPING GUIDE
FOR LEMO CONNECTOR WIRING

FIGURE 4-12. 10 CONDUCTOR CABLE STRIPPING AND WIRE GUIDE



WRAP BACKSHELL WIRING WITH RUBBER TAPE

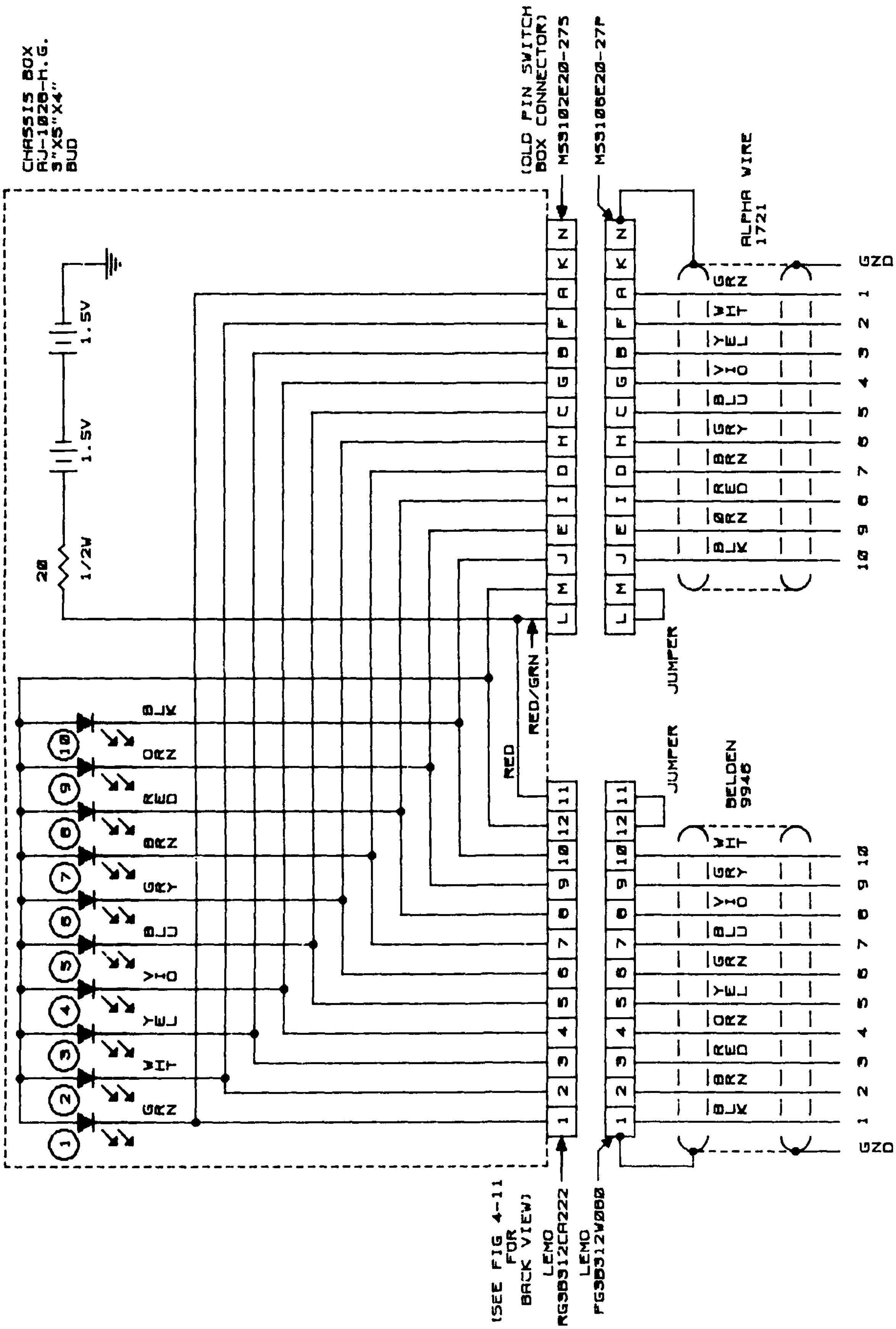
FIGURE 4-13. PIN SWITCH PROBE CABLE SAFETY SHORTING PLUG

TABLE 4-2. PIN SWITCH CIRCUITS INSTRUMENT PARTS LIST

QUANTITY	ITEM	DESCRIPTION/MFR	SOURCE
Resistor, 1% metal film RN55D			
4	100 ohms		servmart
4	200 "		"
4	301 "		"
4	402 "		9ND 5905-00-270-1293
2	499 "		9ND 5905-00-432-0420
2	1k "		servmart
2	10k "		"
2	100k "		"
Resistor, 1/4 watt, 5%, carbon			
11	100 ohms		"
1	200 "		"
1	330 "		"
1	560 "		"
15	1k "		"
2	1.1k "		"
1	4.7k "		"
1	5.1k "		"
1	6.8k "		"
3	10k "		"
1	12k "		"
1	15k "		"
1	470k "		"
11	1M "		"
11	20M "		"
Resistor, 1/2 watt, 5%, carbon			
1	510 ohm		"
Resistor network			
2	560k, bussed, 8 pin, 4608X-101-564,		Bourns
Capacitors			
13	.001MFD	CKR05 series	servmart
10	1500PFD	" "	"
3	.01MFD	" "	"
14	.1MFD	" "	"
2	.47MFD	" "	"
1	1MFD, 25Vdc, ceramic		"
1	1MFD, 50Vdc, Tantalum		"
7	10MFD, 50Vdc, Tantalum		"
2	1-5 PFD, as needed		"
Semiconductors			
11	GA300	silicon controlled rectifier,	Unitrode
1	2N3906	transistor	servmart
1	7815	positive voltage regulator	"
1	7915	negative voltage regulator	"
1	HA2540	operational amplifier,	Harris Semiconductor
3	1N3611	diode	servmart
10	1N914	diode	"

TABLE 4-2.(Cont.)

QUANTITY	ITEM	DESCRIPTION/MFR	SOURCE
2	1N4747A	Zener diode, 20 volt	"
1	1N4728	Zener diode, 3.3 volt	"
1	2N5060	silicon controlled rectifier	"
1	VN10KM	transistor, Siliconix,	9ND 5961-01-123-5416
Integrated circuits			
6	4001	Quad 2-input NOR gate	servmart
2	4013	Dual D FLIP-FLOP	"
1	4017	DECADE COUNTER	"
2	4068	8-input NAND gate	"
1	4071	Quad 2-input OR gate	"
1	4098	Dual MULTIVIBRATOR	"
Hardware			
2		6P2T relay, NL6EX-DC12V,	Aromat Corp
1		ribbon cable plug,7P16-3T12-1,	Augat
2		6 pin DIP sockets	servmart
13		14 pin DIP sockets	servmart
128 pins		0.1" socket strip, 20 pins/strip, SS-120-G2, Samtec,	9ND 5935-01-150-3508
16 pins		0.1" interconnect strip, 20 pins/strip, BBS-132-T-D,	Samtec
2		screw, 6-32 X 1/4	servmart
1		1" standoff, metal, 6-32 internal thread, both ends	"
4		fuseclips, PCB mount, Littlefuse	9ND 5999-00-975-6265
1		single-width module, 040-0652-05,	Tektronix
1		1/4 3AG fuse	servmart
1		1/10 3AG fuse	"
1		15 pin D connector, socket	"
2		latching blocks for D connector, SD-LB,	TRW
1		BNC connector, isolated, chassis	servmart
2		BNC connector, chassis	"
1		LED, red, MV5153, with socket	9ND 5961-01-016-8137
1		3X4 keyboard switch, 83AC1-101,	Grayhill
1		printed circuit board, pin switch	NSWC E132
1		printed circuit board, test circuit	NSWC E132
1		front panel	NSWC E132
Cable Connector and Transfer Box Assembly			
15ft		15 conductor cable, 9541,	Belden
1		15 pin D connector, plug	9ND 5935-00-975-6265
1		hood adaptor for 15 pin D conn, SDH-15BL	TRW
2		12 pin connector, chassis, RG3B312CA222,	Lemo
1		12 pin connector, cable plug, FG3B312W080,	Lemo
25ft		10 conductor cable, 9946,	Belden
25ft		10 conductor cable, 9946	Belden
1		3X4X5 alum box, AU-1028-H.G., Bud	servmart
1		BNC connector, chassis	servmart
1		BNC connector, cable	"
25ft		RG58 coaxial cable	"



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